A Resonant DC Link Inverter for an Electric Vehicle

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the requirements for the Degree of Master of Engineering
(Electrical and Electronic)

at the
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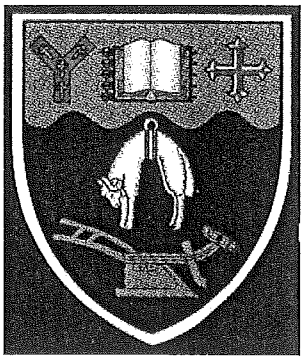

by
Zhenyue Hong, B.E.

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ABSTRACT

Voltage source PWM inverters have been the main choice in electric vehicles, because of circuit simplicity and rugged control schemes. The inverters, however, suffer from high switching losses, high switching stresses, and EMI problems. Resonant DC link inverters have been actively considered by many manufacturers for industrial applications, in order to achieve better performance, higher efficiency, and higher power density.

This thesis presents the design, implementation, and test results of a resonant DC link inverter for an electric vehicle application. The resonant DC link inverter operates off a 240V DC supply, and drives a 2.2kW induction motor. The link frequency is approximately 70kHz. The resonant inverter uses 600V IGBT devices with an active clamping circuit limiting the bus voltage below 500V. A synchronized PWM scheme, in which, the conventional PWM switching signals are synchronized to zero crossings of the resonant bus voltage, is used to modulate the resonant inverter.

Operating principles, detailed analyses, and simulations are presented, followed by power loss calculations and a design optimization to find the optimal values of the resonant components. The construction of the resonant inverter with the emphasis on minimizing stray inductance is described. A resonant link control circuit for maintaining resonant operation and limiting the bus voltage is developed. Experimental tests demonstrate the successful operation of the resonant inverter with the induction motor under a rated load, and the capability of bidirectional power flow is confirmed. Loss measurement shows that under the identical load conditions and for the same IGBT devices, the resonant inverter has a 78% reduction of the switching losses in the main devices and a 20% reduction of the total losses in comparison to the conventional voltage source PWM inverter operating at a PWM switching frequency of 14kHz.

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CHAPTER 1

INTRODUCTION

In response to concerns about energy cost and environment damage, a rekindling of interest in electric vehicles (EVs) has been obvious. Based on the "California rules" on zero emission vehicles in the United States, as well as similar tightened air pollution regulation in Europe, Asia, and much of the rest of the world, the market for electric vehicles has been growing. The development of power electronics technology for electric vehicles has been taking an accelerated pace to fulfill the market needs.

Electric propulsion, a major power electronics area, plays a very important role in electric vehicles. A power converter is used to regulate power flow between batteries and the EV propulsion motor. To maximize the usage of battery energy the power converter should have a high efficiency and a capability of bidirectional power flow. An extra 1% efficiency in EV propulsion can enable an additional few miles in the EV driving range, and the generated energy from the motor due to frequent deceleration can normally extend the driving range up to 25% [Chan, 1997].

The University of Canterbury has been involved in electric vehicle development since 1974. The main motivation has been to provide a suitable test-bed by which to demonstrate drive systems, control systems and various other systems. The University's vehicle is powered by twenty series connected 12V lead acid batteries to give a nominal 240V DC supply. The supply voltage can vary from 280V with the batteries fully charged to 180V with the batteries exhausted. The University's vehicle is driven by two three-phase induction motors linked to two rear wheels by chain drives. The induction motors have been specially rewound to allow them to operate off a lower supply voltage. Each induction motor has a rated power of 2.2kW, a rated line-to-line voltage of 90V rms, and a rated frequency of 50Hz. The induction motors

are capable of delivering a maximum continuous power of 6kW and can deliver up to 11kW for short periods [Williams M., 1993].

1.1 Hard Switching Inverter

Usually electric vehicles utilize voltage source PWM (Pulse-Width Modulated) inverters, as shown in Figure 1.1, to convert DC power from a battery bank into AC power for driving induction motors. In this circuit the power devices are connected to a constant voltage source, thus this circuit is also termed as a hard switching inverter.

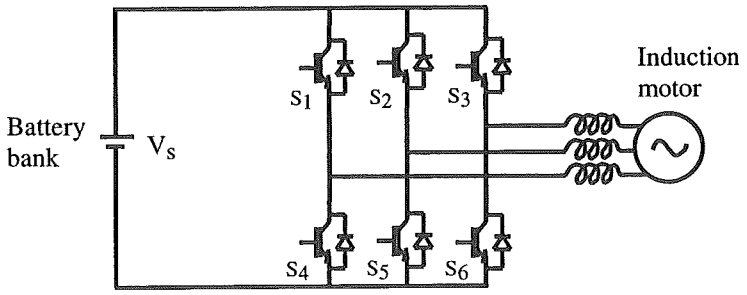


Figure 1.1. Circuit schematic of a hard switching PWM inverter.

The attractiveness of this topology stems from its extremely simple power structure. The control is reasonably simple and provides a fully regenerative interface between DC source and AC induction motor. However, the following problems can be identified with this topology [Divan, 1989a] [Divan, 1997].

- Switching losses result from sudden changes in device voltage and current waveforms, and the switching losses increase significantly with PWM switching frequency.
- Switching stresses (high current and high voltage spikes) on the device during the turn-on and turn-off transients require large SOA (Safe Operating Area) specifications and compromise reliability.
- High di/dt and dv/dt generate electromagnetic interference (EMI).
- High dv/dt generates high voltage spikes at the motor terminals and these spikes may cause insulation failure of the motor winding when the motor is connected to the inverter using a long cable.

Due to these limitations the PWM switching frequency in the hard switching inverter is usually around a few kilohertz when the inverter power rating is tens of kilowatts

[Bellar, 1998]. Therefore, power density and circuit performance of the hard switching inverter are limited with a low PWM switching frequency.

In the late 1980's and early 1990's, new soft switching resonant inverter topologies such as the resonant DC link inverter and the actively clamped resonant DC link inverter were introduced by Divan [Divan, 1989a] [Divan, 1989b]. In the resonant DC link inverter, a high frequency resonant network is added to a conventional voltage source PWM inverter. As a result, the bus voltage swings and crosses zero and, thus, creates zero voltage switching conditions (i.e., so-called soft switching) for the power devices. Therefore, switching losses can be minimized, switching stresses can be reduced, and EMI can be prevented. Further, the use of the resonant DC link can reduce the dv/dt of the inverter output voltage and suppress the voltage overshoot at the motor terminals [Suh, 1996]. The resonant DC link inverter has been shown a viable topology to realize high performance, high power density DC/AC inverters [Mertens, 1990]. The application of the resonant DC link inverter has been actively considered by many manufacturers. Such inverters are now commercially available at power ratings up to 200kVA at 480V input, and these commercial units have advantages of high efficiency, less severe EMI problems, very low acoustic noise, snubberless operation, and improved reliability [www.softswitch.com].

1.2 Project Outline

This thesis looks at the development of a resonant DC link inverter for an electric vehicle application. The main objectives are to demonstrate bi-directional operation of the resonant inverter, and investigate whether the resonant inverter is more efficient than a conventional hard switching PWM inverter.

Chapter 2 of this thesis describes the operating principles of the resonant DC link inverter. Chapter 3 presents a simulation study of the resonant inverter with a three-phase load. In Chapter 4, power losses in the resonant DC link inverter are estimated, and the optimal values of resonant components are determined. The components and construction of a prototype resonant DC link inverter are described in Chapter 5. Chapter 6 details the design of a resonant link control circuit. Experimental results

are presented in Chapters 7, 8 and 9. Chapter 7 describes the tests of the resonant inverter under no-load. Chapter 8 presents experimental results of the resonant inverter operated with an inductive load and an induction motor. A performance evaluation is given in Chapter 9, where the measured results of the power losses and the THD (Total Harmonic Distortion) of the motor current in the resonant inverter are compared with those obtained using a conventional hard switching PWM inverter. Chapter 10 gives a suggestion for future work, and Chapter 11 concludes this thesis.

CHAPTER 2

OPERATING PRINCIPLES AND ANALYSES

This chapter describes the operating principles of a resonant DC link inverter (RDCLI). The minimum trip current required to ensure resonant operation and the bus overvoltage associated with resonant operation are analyzed. Then, an actively clamped resonant DC link inverter (ACRLI) suitable for the electric vehicle application is introduced. The operating principles of the actively clamped resonant DC link inverter are described, and detailed analyses of the actively clamped resonant DC link inverter under no-load and load conditions are presented.

2.1 Resonant DC Link Inverter

The resonant DC link inverter was the first soft switching inverter reported in the literature [Divan, 1989a], and represented the beginning of significant research activity worldwide in this field. Figure 2.1 shows the circuit schematic of the resonant DC link inverter. In this circuit, a resonant network composed of one small inductor and capacitor is added to the DC bus of a conventional voltage source PWM

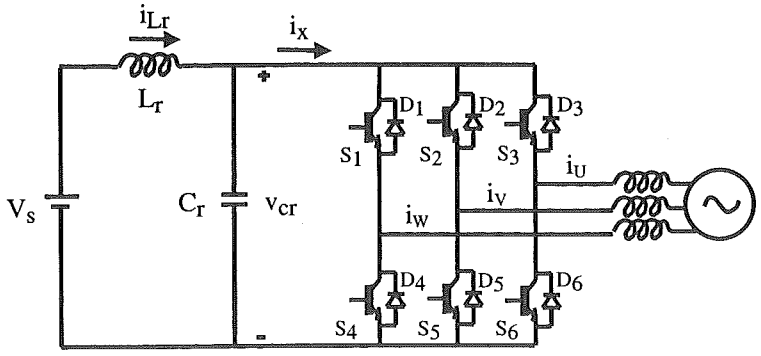


Figure 2.1. Circuit schematic of the resonant DC link inverter.

inverter. The voltage across the resonant capacitor, C_r, is also impressed across the six devices in the inverter stage. The average or DC value of this voltage equals that of the supply voltage, and superimposed on the supply voltage is an oscillating or resonant component. The combined voltage is referred to as the resonant bus voltage, v_{cr}. The resonant link is excited and maintains resonance through the control of the inverter devices so that the resonant bus voltage reaches zero volts periodically. Switching of the inverter devices is synchronized to the resonant voltage's zero crossings so as to obtain the low loss switching.

2.1.1 Operating Principle

Consider the circuit in Figure 2.1 with lossless link components, L_r and C_r. If the supply voltage V_s is applied to the resonant link with the inverter stage disconnected, the resonant bus voltage, v_{cr}, will be given by Equation 2.1.

$$v_{cr}(t) = V_s(1 - \cos \omega t) \tag{2.1}$$

In Equation 2.1, ω is the angular frequency of the L_r-C_r tank, and is given by Equation 2.2.

$$\omega = \frac{1}{\sqrt{L_r C_r}} \tag{2.2}$$

At $\omega t = 2\pi$, the resonant bus voltage will return to zero volts, thus setting up the desired switching condition. For a lossy L_r-C_r tank, the bus voltage will never return to zero and will stabilize at V_s. However, if six devices in the inverter stage are maintained on while applying V_s, the resonant inductor current, i_{Lr}, is seen to increase linearly. When sufficient energy is stored in the resonant inductor to ensure that the bus voltage returns to zero, all the devices are then operated according to the PWM switching signals. Once the bus voltage returns to zero volts, all the devices can be turned on again so as to repeat the process and establish the resonant operation. Having established the desired resonant operation, the duration of zero bus voltage is then used to accomplish low loss switching of all the devices across the bus.

Clearly, the control of the six devices of the inverter stage will need modification from the standard PWM strategy to include the charging control of the resonant inductor. Furthermore, since the bus voltage is periodic, and the inverter devices are only switched during the zero voltage intervals, the low frequency output voltage has to be synthesized using integral cycles of the resonant bus voltage.

2.1.2 Equivalent Circuit

For the analysis of the resonant DC link inverter, the equivalent circuit shown in Figure 2.2a is used. The resistance, R_S, defines the quality factor of the resonant link. Switch S_m (D_m) and a controlled current source i_X represent the inverter stage. i_X is the inverter DC current given by Equation 2.3.

$$i_X = i_u \cdot S_u + i_v \cdot S_v + i_w \cdot S_w \qquad (2.3)$$

In Equation 2.3, i_u, i_v and i_w are the phase currents of the load, and S_u, S_v and S_w are the switching functions of the inverter. Given a PWM-type modulation for the inverter stage, the inverter DC current can vary by a large amount from one PWM switching cycle to the next as illustrated in Figure 2.2b. However, during one resonant cycle itself, the inverter DC current remains virtually constant, assuming that the load current is slowly varying and the PWM switching frequency is much lower than the resonant frequency.

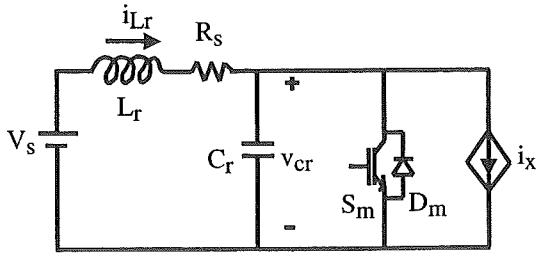


Figure 2.2a. Equivalent circuit of the resonant DC link inverter.

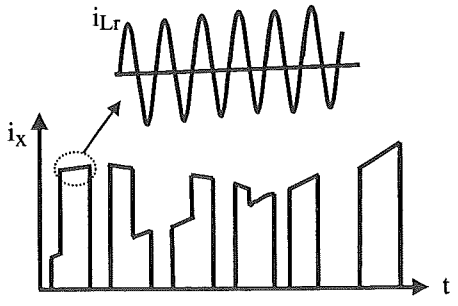


Figure 2.2b. Typical waveform of the inverter DC current.

2.1.3 Minimum Trip Current

In Figure 2.2a, if switch S_m is turned off when the initial current in the resonant inductor is $i_{Lr}(0)$, and the inverter DC current has a constant value of I_X, the bus voltage and inductor current for the duration of one resonant cycle can be determined from Equations 2.4 and 2.5 [Divan, 1989a].

$$v_{cr}(t) = V_S + e^{-\alpha t}[-V_S \cdot \cos \omega t + Z_r \cdot I_T \cdot \sin \omega t] \tag{2.4}$$

$$i_{Lr}(t) = I_X + e^{-\alpha t}[I_T \cdot \cos \omega t + \frac{V_S}{Z_r} \cdot \sin \omega t] \tag{2.5}$$

where:

$$I_T = i_{Lr}(0) - I_X \tag{2.6}$$

$$Z_r = \sqrt{\frac{L_r}{C_r}} \tag{2.7}$$

$$\alpha = \frac{R_S}{2L_r} \tag{2.8}$$

Z_r in the above equations is termed as the resonant impedance of the resonant link, and I_T, the difference between the initial inductor current and the inverter DC current at the beginning of the resonant cycle, is defined as the trip current.

It can be shown from Equation 2.4 that the additional term associated with the trip current is necessary to make v_{cr} to return to zero after one resonant cycle. The return to zero of v_{cr} is essentially independent of the inverter DC current I_X and is strongly dependent on the trip current I_T. This implies that the resonant operation can be maintained even with a negative inverter DC current, as would happen when the inverter operates with an induction motor in regeneration mode.

To maintain resonant operation the current difference (i_{Lr}-I_X) must be monitored when S_m is conducting, and S_m is turned off when (i_{Lr}-I_X) equals a minimum value. However, the inverter DC current changes from one PWM switching cycle to the next as shown in Figure 2.2b. This necessities a control circuit (to be described in Section

6.1) to predict the inverter DC current, thereby setting up a proper initial current in the resonant inductor at the beginning of each resonant cycle.

A detailed analysis [Schulting, 1992] shows that the minimum trip current $I_T(min)$, below which the bus voltage will not return to zero after one resonant cycle, is given by Equation 2.9.

$$I_T(min) = \sqrt{\frac{2\pi}{Q}}\frac{V_S}{Z_r} \tag{2.9}$$

In Equation 2.9, Q is the quality factor of the resonant inductor. Clearly, the minimum trip current is dependent on the quality of the resonant inductor and the peak resonant current, V_S/Z_r. For a realistic quality factor of 190, the minimum trip current is about 20% of the peak resonant current.

2.1.4 Bus Overvoltage

Assuming that the resonant link is highly under-damped, i.e., R_S=0, Equations 2.4 and 2.5 can be simplified further as given in Equations 2.10 and 2.11.

$$v_{cr}(t) = V_S + [-V_S \cdot \cos\omega t + Z_r \cdot I_T \cdot \sin\omega t] \tag{2.10}$$

$$i_{Lr}(t) = I_X + [I_T \cdot \cos\omega t + \frac{V_S}{Z_r} \cdot \sin\omega t] \tag{2.11}$$

From Equation 2.10, it is seen that the average value of the bus voltage for one resonant cycle equals the supply voltage. From Equation 2.11, the inductor current has two identifiable components; the inverter DC current and the AC circulating current. The instantaneous power supplied from the DC source is composed of the active power delivered to the load and the reactive power required for sustaining the link resonance.

As illustrated in Figure 2.2b, the use of a PWM-type modulation may cause a very rapid decrease in the inverter DC current. The resulting difference between the inductor current and the inverter DC current over-excites the resonant link causing large overshoots in the bus voltage. Differentiating Equation 2.10, the peak bus voltage can be found and is expressed by Equation 2.12.

$$V_{cr}(pk) = V_S[2 + 0.5 \cdot (\frac{Z_r I_T}{V_S})^2] \quad (2.12)$$

For an extreme case when the inverter DC current decreases rapidly from a peak load current $I_o(pk)$ to zero, the trip current I_T in Equation 2.12 is equal to $I_o(pk)$. If $I_o(pk)$=30A, Z_r=9.35Ω, and V_S=240V, then the peak bus voltage $V_{cr}(pk)$ may be as high as 640V. Moreover, the bus voltage may be much higher during regeneration when the inverter DC current reverses and flows back to the DC source.

Any overvoltage of the resonant bus occurring in the resonant DC link inverter (Figure 2.1) must be limited to an acceptable level for the inverter devices. Many methods have been proposed in the literature for this purpose, such as the actively clamped resonant DC link [Divan, 1989b], the passively clamped resonant DC link [Skibinski, 1993], the reduced voltage resonant link [Deshpande, 1996], and voltage peak control [Nielsen, 1996]. Among them, the actively clamped resonant DC link is preferred owing to its excellent clamping performance and ease of implementation. The actively clamped resonant DC link inverter is analyzed next.

2.2 Actively Clamped Resonant DC Link Inverter

Figure 2.3 shows the circuit schematic of an actively clamped resonant DC link inverter. An auxiliary device (S_c and D_c) and a capacitor (C_c) are added to the original resonant DC link inverter (Figure 2.1). The clamp capacitor, C_c, and the DC source provide a clamping voltage, KV_S. The voltage across the clamp capacitor is $(K-1)V_S$, where K is referred to as the clamping ratio. The clamp capacitor needs to be precharged before the link resonance is initiated. The circuit for precharging the clamp capacitor is described in Section 6.4.1. With the active clamping, the peak resonant voltage can be limited to 1.3 to1.8 times of the supply voltage [Divan, 1989b].

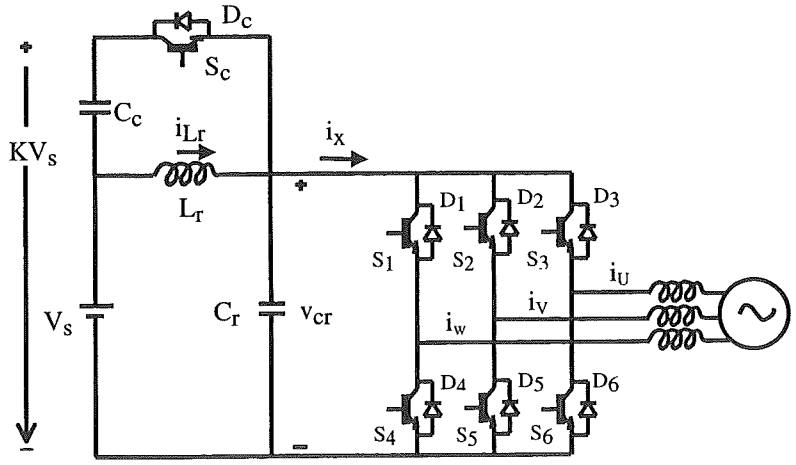


Figure 2.3. Circuit schematic of the actively clamped resonant DC link inverter.

2.2.1 Operating Principle

In a manner similar to the original resonant DC link inverter, the resonant bus is shorted to allow the resonant inductor to be charged. On releasing the bus shorting, the bus voltage resonates towards its natural peak. On reaching the clamping voltage KV_S, diode D_C turns on and clamps the bus voltage. With D_C conducting, the device S_C is turned on in a lossless manner. The current eventually transfers from the diode D_C to the device S_C. The charge transferred to the clamp capacitor C_C with D_C conducting is recovered during the interval when S_C conducts. When the net charge transferred to C_C equals zero, S_C is turned off, and the L_r-C_r circuit continues to resonate until the bus voltage reaches zero volts. At this point the resonant cycle can be reinitiated as required.

It is clear that by using the active clamping the bus voltage can be restricted to the clamping voltage KV_S while maintaining resonant operation similar to the original resonant DC link inverter, if a pre-cycle charge balance is ensured. When the resonant inverter is under load the charge flowing into the clamp capacitor changes with the inverter DC current. The charge removed from the clamp capacitor changes with the conduction time of S_C. Thus it seems to be a difficult task to ensure the

charge balance on a per-cycle basis. However, if the clamp capacitance is large enough, the charge balance over a few resonant cycles is possible given a constant conduction time of S_c, and consequently the clamping voltage can be maintained [Divan, 1993]. The clamping voltage, KV_s, can be set as required through the control of the conduction time of S_c. The circuit for the active clamping control is detailed in Section 6.2.

2.2.2 Operation under no Load

Under no-load conditions, the actively clamped resonant DC link inverter can be analyzed using the simplified circuit shown in Figure 2.4a, and the associated current and voltage waveforms are given in Figure 2.4b.

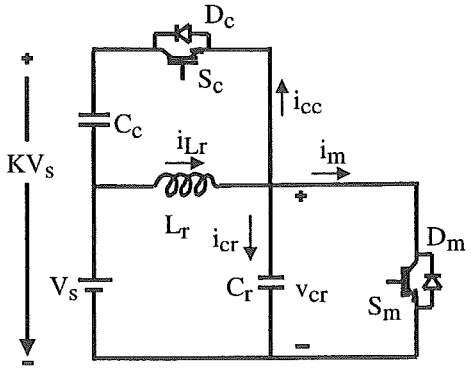


Figure 2.4a. Simplified circuit for the ACRLI under no-load.

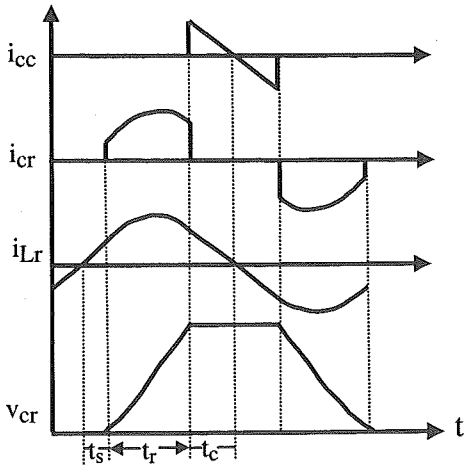


Figure 2.4b. Waveforms for the ACRLI under no-load.

If lossless components and a per-cycle charge balance are assumed then the bus voltage, v_{cr}, and inductor current, i_{Lr}, waveforms are symmetrical. Three different phases in one half cycle can be identified. The resonant cycle is started with the charging of the resonant inductor through the main device, S_m. At the end of a charging time, t_s, the inductor current, i.e., the trip current I_T under the no-load conditions, can be expressed by Equation 2.13.

$$I_T = \frac{V_S}{L_r} t_S \qquad (2.13)$$

After turn-off of S_m, LC resonance takes place. The bus voltage and inductor current can be expressed using Equations 2.14 and 2.15.

$$v_{cr}(t) = V_S(1-\cos\omega t) + Z_r \cdot I_T \cdot \sin\omega t \tag{2.14}$$

$$i_{Lr}(t) = I_T \cdot \cos\omega t + \frac{Vs}{Z_r} \cdot \sin\omega t \tag{2.15}$$

After a resonant transition time, t_r, the bus voltage reaches the clamping voltage. Solving Equation (2.14) with the constraint $v_{cr}(t_r) = KV_S$, the transition time t_r can be found and is given in Equation 2.16.

$$t_r = \frac{1}{\omega}\left[a\sin\left(\frac{(K-1)V_S}{\sqrt{(Z_r I_T)^2 + {V_S}^2}}\right) + a\sin\left(\frac{V_S}{\sqrt{(Z_r I_T)^2 + {V_S}^2}}\right)\right] \tag{2.16}$$

At the same time the clamp diode, D_c, starts to conduct. The peak current flowing through D_c can be found using Equation 2.17.

$$I_{ccp} = \sqrt{{I_T}^2 + (2K - K^2)\left(\frac{V_S}{Z_r}\right)^2} \tag{2.17}$$

The time needed to demagnetize the resonant inductor, t_c, is given by Equation 2.18, and forms the third phase of one half resonant cycle while $v_{cr}(t)=KV_S$.

$$t_c = \frac{L_r I_{ccp}}{(K-1)V_S} \tag{2.18}$$

The resonant frequency, f_r, can then be found by summing the total time intervals associated with one resonant cycle, and is given by Equation 2.19.

$$f_r = \frac{1}{2(t_s + t_r + t_c)} \tag{2.19}$$

The resonant capacitor current equals zero during the voltage clamping and the bus shorting intervals, and equals inductor current during link resonance as shown in Figure 2.4b. The rms current in the resonant capacitor, I_{cr}(rms), can be obtained by using Equation 2.20 [Mertens, 1990].

$$I_{cr}(\text{rms}) = \sqrt{t_r f_r [I_T{}^2 + (\frac{V_s}{Z_r})^2]} \tag{2.20}$$

The clamp device (D_c and S_c) operates at the resonant frequency, and its current has a high di/dt level. This implies that the performance of the active clamping is very sensitive to the stray inductance in the clamping path. The rms current of the clamp device, I_{cc}(rms), can be determined using Equation 2.21.

$$I_{cc}(\text{rms}) = \sqrt{f_r \frac{2(K-1)^2 V_s{}^2 t_c{}^3}{3L_r{}^2}} \tag{2.21}$$

Similarly, the rms current in the resonant inductor current, I_{Lr}(rms), can be obtained and is given by Equation 2.22.

$$I_{Lr}(\text{rms}) = \sqrt{I^2{}_{cr}(\text{rms}) + f_r \frac{2V_s{}^2 t_s{}^3}{3L_r{}^3} + f_r \frac{2(K-1)^2 V_s{}^2 t_s{}^3}{3L_r{}^2}} \tag{2.22}$$

The resonant frequency and component currents are seen to be fairly sensitive to the design parameters. Based on the above equations, calculations are performed for the actively clamped resonant DC link under no-load, using the parameters, V_s=240V, L_r=20.45μH, and C_r=0.234μF, and the results are shown in Figures 2.5 and 2.6. It can be seen from Figure 2.5 that the rms currents in the inductor and the clamp device increase with the increase of the inductor charging time t_s. Changing t_s by as little as one microsecond can causes I_{Lr}(rms) and I_{cc}(rms) to go up by about 10% and 70%, respectively, while the current in the resonant capacitor stays almost constant.

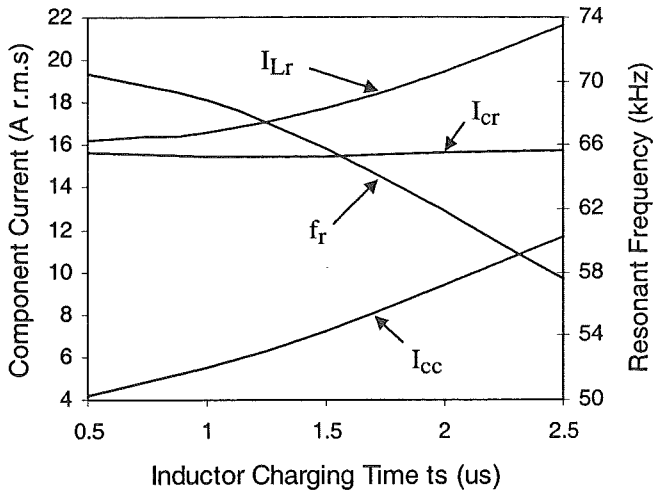


Figure 2.5. Variation of the resonant frequency and component currents with the inductor charging time t_s.

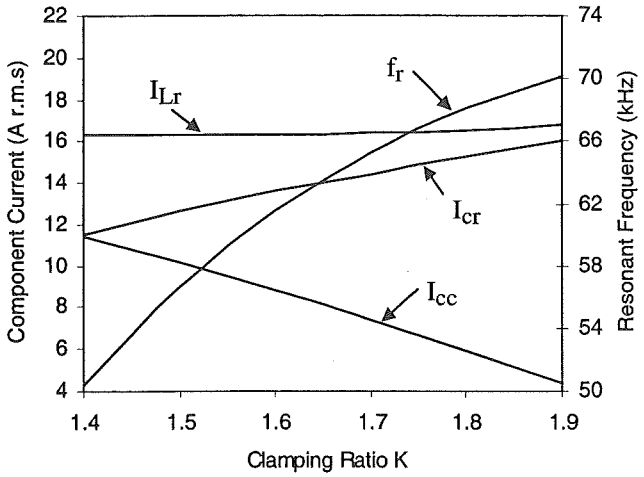


Figure 2.6. Variation of the resonant frequency and component currents with the clamping ratio K.

As shown in Figure 2.6, the current in the resonant capacitor is very strongly dependent on the clamping ratio K. A lower value of K suggests that more energy is diverted to the clamp capacitor, thus there is a higher rms current in the clamp device and a lower rms current in the resonant capacitor. The rms current in the inductor remains almost constant with the change of the clamping ratio. Besides the values of the resonant components, L_r and C_r, the parameters K and t_s strongly influence the resonant frequency, as depicted in Figures 2.5 and 2.6.

2.2.3 Operation under Load

When the resonant DC link inverter operates with a load, the inverter DC current flows through the resonant inductor and also increases the current flowing through the clamp device. Another impact of the load is that the resonant frequency changes with the inverter DC current. The transitions in the inverter DC current depend on the modulation strategy adopted for the output control of the inverter. As for a synchronized PWM strategy, to be discussed in Section 6.1.4, the transitions of the inverter DC current, from zero to the peak load current $I_o(pk)$ and from the peak load $I_o(pk)$ to zero, can be considered as the worst cases to estimate the component stresses for the resonant link under the load conditions.

Figure 2.7 illustrates the waveforms of the inductor current and bus voltage during the event when the inverter DC current increases from zero to the peak load current $I_o(pk)$. A longer inductor charging time, t_s, is required to ramp the inductor current up to the peak load current plus a minimum trip current $I_T(min)$. Ignoring $I_T(min)$, the time can be found using Equation 2.23.

$$t_s = \frac{I_o(pk)L_r}{V_s} \tag{2.23}$$

The peak current in the resonant inductor is approximately given by the sum of the peak load current and the peak resonant current as given in Equation 2.24.

$$I_{Lr}(pk) = I_o(pk) + \frac{V_s}{Z_r} \tag{2.24}$$

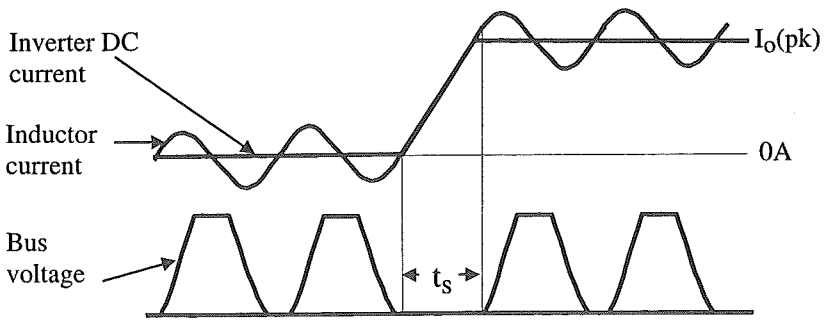


Figure 2.7. Link waveforms when the inverter DC current increases from 0A to $I_o(pk)$.

The second case when the inverter DC current decreases from the peak load current $I_o(pk)$ to zero is illustrated in Figure 2.8. In this case, the trip current at beginning of the resonant cycle equals the peak load current, $I_o(pk)$, and no charging time is required. This excessive trip current causes the bus voltage to rise rapidly. The peak current in the clamping device can be determined using Equation 2.25

$$I_{ccpl} = \sqrt{I_o(pk)^2 + (2K - K^2)(\frac{V_s}{Z_r})^2} \tag{2.25}$$

A longer clamping time, t_c, is required to transfer excessive energy from the resonant tank to the clamp capacitor as given in Equation 2.26.

$$t_c = \frac{L_r I_{ccpl}}{(K-1)V_s} \tag{2.26}$$

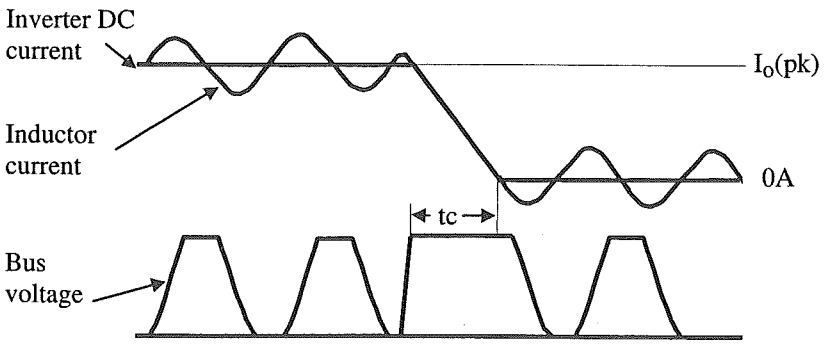


Figure 2.8. Link waveforms when the inverter DC current decreases from $I_o(pk)$ to zero.

A more serious situation may occur, when the resonant inverter operates with an induction motor, and the inverter DC current reverses due to the mode change from motoring to regenerating. The peak current flowing through the clamp device may be larger than that given by Equation 2.25.

2.3 Summary

This chapter has analyzed two resonant inverter topologies; namely, the resonant DC link inverter and the actively clamped resonant DC link inverter. The difference between the resonant inductor current and the inverter DC current at the beginning of a resonant cycle (i.e., the trip current) determines whether the resonant bus voltage will return to zero after the resonant cycle. The minimum trip current to sustain the link resonance is determined by the quality factor of the resonant inductor. In the resonant DC link inverter, a bus overvoltage may occur when the inverter DC current decreases. It is estimated that the peak bus voltage may reach 640V in the resonant DC link inverter for the electric vehicle application. In addition, the control of the inverter stage needs modification to include the control of the resonant link and perform the inverter modulation with the discrete pulses of the resonant bus voltage.

In the actively clamped resonant DC link inverter, the peak bus voltage can be limited to 1.3 to 1.8 times of the supply voltage by controlling the conduction time of the clamp device. Current stresses in the link components are very sensitive to the link parameters such as the inductor charging time and clamping ratio. When the resonant inverter operates with a load, the resonant frequency varies with the change in the inverter DC current. A longer bus-shorting period is required to charge the resonant inductor when the inverter DC current increases. A longer voltage-clamping period is required to transfer excessive energy from the resonant tank to the clamp capacitor when the inverter DC current decreases. To investigate the details of the actively clamped resonant DC link inverter for the electric vehicle application, a simulation study is performed and is presented in the next chapter.

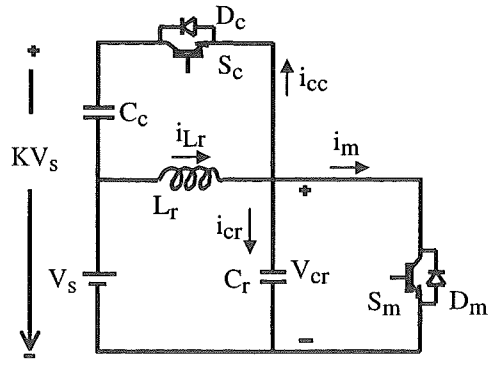
CHAPTER 3

SIMULATIONS

This chapter describes the simulations of the actively clamped resonant DC link inverter. Simulation waveforms showing the operation of the resonant inverter in motoring and regenerating modes are given. Component stresses of the actively clamped resonant DC link inverter operating with a typical load are evaluated. The impacts of the stray inductance on the operational behavior of the resonant inverter are investigated.

3.1 Resonant Link

The simplified actively clamped resonant DC link as shown in Figure 3.1 was simulated using PSpice. The DC source was assumed to be constant and ripple free, and the passive components, L_r, C_r and C_c, were assumed to be ideal. The main device (S_m, D_m) and the clamp device (S_c, D_c) were modeled with an IGBT model BSM50GB100G (50A/1000V) and a diode model MUR1650 (16A/600V, Ultrafast). These simulation models were chosen as they have the closest ratings to that of the



Resonant inductor L_r=20.45μH

Resonant capacitor C_r=0.234μF

Clamp capacitor C_c=2200μF

DC source V_s=240V

Clamping voltage KV_s=440V

Figure 3.1. Simulation circuit for the actively clamped resonant DC link.

devices used for this project, and they are available in the PSpice library. The parameters used for the simulation are listed beside Figure 3.1. The initial voltage of the clamp capacitor was set to 200V, giving a clamping voltage KV_S of 440V.

Typical simulated waveforms are shown in Figure 3.2 for an inductor charging time t_S of 1.5μs, and this corresponds to a trip current I_T of 17.6A in the resonant inductor. Given ideal link components, the simulated waveforms are same as those analyzed in the previous chapter (Figure 2.4b). Furthermore, the simulation results of the resonant frequency, time periods associated with the resonant cycle, and the various component currents are exactly same as the calculated results using Equations 2.13 to 2.22. Therefore the validity of these equations is verified.

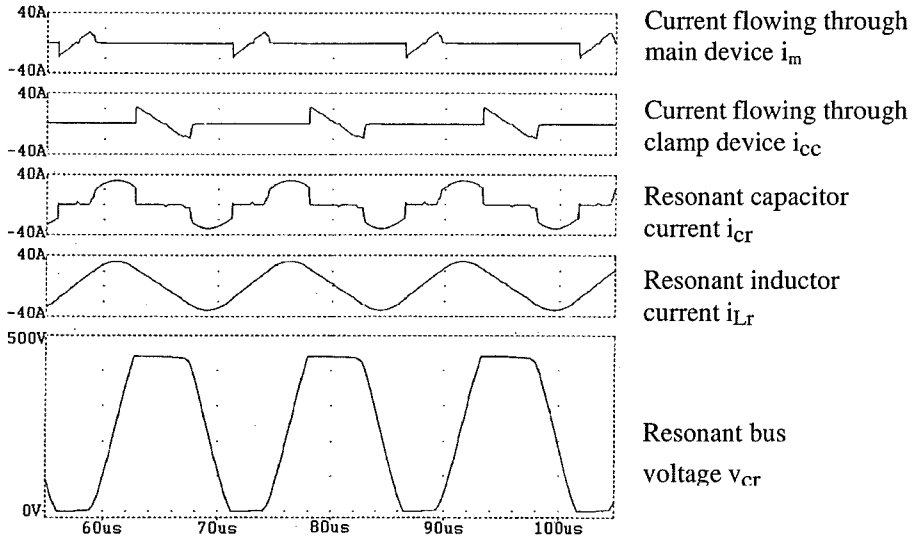


Figure 3.2. Simulated waveforms of the actively clamped resonant DC link with ideal components.

3.2 Resonant Inverter

Simulations were performed for the actively clamped resonant DC link inverter with a three-phase load shown in Figure 3.3. The load was simply assumed to be a three-phase sinusoidal current source with a current rating of 25A rms at 50Hz, which is expected for driving a 2.2kW induction motor in the electric vehicle application. The link components were again assumed to be ideal, the inverter devices S_1-S_6 and D_1-

D_6 were simulated using the IGBT model BSM50GB100G and the diode model MUR1650, respectively.

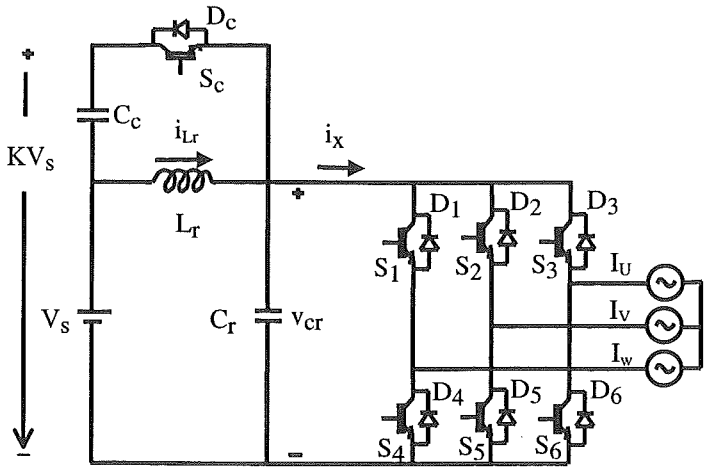


Figure 3.3. Simulation circuit for the actively clamped resonant link inverter with a three-phase load.

In the resonant DC link inverter, the low frequency output voltage must be synthesized using integral pulses of the resonant bus voltage. A synchronized PWM scheme was used to modulate the inverter throughout the simulations. In this scheme, the sinusoidal PWM signals, generated by comparing a triangular waveform with a sinusoidal reference waveform, are synchronized to the zero crossing of the bus voltage in order to achieve zero voltage switching. By specifying a lagging or leading phase angle between the load current and the PWM reference signal, the load can be modeled so as to consume or generate power, simulations for the resonant inverter operating in motoring and regenerating modes can then be performed.

As mentioned before, when the resonant inverter operates with a three-phase load, the resonant link can be subjected to severe inverter DC current transitions. To meet the proper initial condition in the resonant inductor, it is necessary to predict the inverter DC current for the next resonant cycle prior to the zero crossing of the bus voltage. The predicted value of the inverter DC current, I_X^*, is obtained by knowing the load phase currents and the status of the inverter switches to be updated. This predicted value is then supplied to a control circuit, which establishes the required initial current

in the resonant inductor [Deshpande, 1997]. The current-prediction scheme is further detailed in Section 6.1

Figure 3.4 shows the simulated waveforms of the resonant inverter operating in the motoring mode. As it can be seen that the resonant link operates satisfactorily even when the inverter DC current undergoes frequent changes. When the inverter DC current increases, the time required for the charging of resonant inductor becomes longer. When the inverter DC current decreases, however, no inductor charging time is required, but the voltage clamping time becomes longer. With the use of an ideal active clamping no overshoot is observed in the bus voltage when the inverter DC current decreases abruptly, the peak bus voltage is limited to the clamping voltage of 440V, reducing the voltage stresses on the inverter devices.

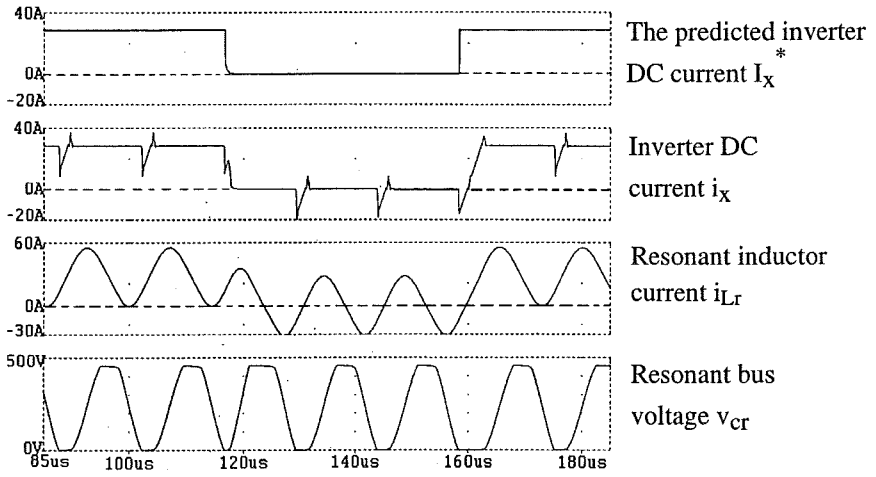


Figure 3.4. Simulated waveforms of the actively clamped resonant DC link inverter operating in motoring mode.

The "saw-tooth" shapes appearing periodically in the waveform of the inverter DC current indicate that all the antiparallel diodes in the inverter stage conduct first and clamp the bus voltage to zero when the bus voltage reaches zero volts, then the switching devices are turned on for the inductor charging. Note that although the inverter devices are involved with maintaining the link resonance, the additional current stresses on these devices are seen to be minimal. Also, it is noted that the changes in the inverter DC current occur only during the zero voltage intervals, demonstrating the zero voltage switchings of the inverter devices.

The top trace in Figure 3.4 is the predicted inverter DC current, I_X^*, which is the reference signal for the inductor charging control (to be described in Section 6.1.3). A close examination of the waveforms of i_X and I_X^* reveals that the predicted inverter DC current changes a little earlier than the actual inverter DC current, demonstrating the operation of the current prediction scheme.

Figure 3.5 shows the simulated waveform of the resonant inverter operating in regenerating mode. It can be seen that the resonant link operates successfully even when the inverter DC current is reversed. Because that the resonant capacitor is periodically reset by resonating with the inductor, the regenerated energy is fed back to the DC source through the resonant link instead of accumulating in the resonant capacitor, as it is clear that the average value of the inductor current is negative. The inverter devices are still switched under the zero voltage switching conditions in the regenerating mode. There is no need to modify the resonant link control circuit to cope with the regenerating operation.

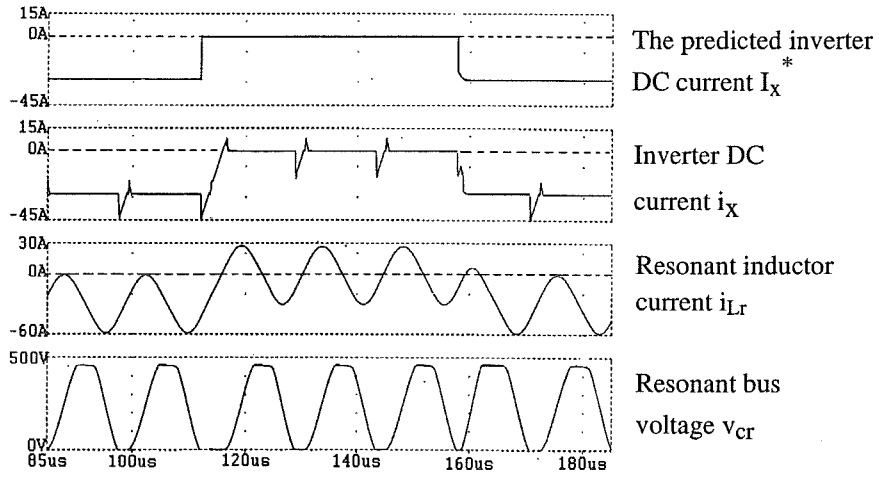


Figure 3.5. Simulated waveforms of the actively clamped resonant DC link inverter operating in regenerating mode.

From both simulations it is verified that the resonant DC link inverter is capable of bidirectional power flow. This important feature makes the resonant DC link inverter more suitable for an electric vehicle application where energy saving is of great concern.

In order to evaluate the current stresses on the various components of the resonant inverter under a typical load, a simulation was undertaken. The simulated circuit was the same as in Figure 3.3, the load phase currents were set to 25A rms at a fundamental frequency of 50Hz, power factor was 0.86, the modulation index of the synchronized PWM signals was set to 0.5, and the clamping voltage was 440V. The simulation was run over an entire output cycle of 20ms. Table 3.1 shows the details of the rms, average, and peak currents on the various components.

Table 3.1 Current Stresses on the Various Components

Component		Current Stresses (A)		
		RMS	Average	Peak
Resonant inductor L_r		25.4	9.8	62
Resonant capacitor C_r		19	0.0	31
Clamp capacitor C_c		5.1	0.0	36
Main devices	S_1-S_6	14.6	7.5	40
	D_1-D_6	10.0	3.8	35.5
Clamp device	S_c	3.8	1.2	28
	D_c	3.7	1.1	36

It is reasonable that the current stresses on all the link components increase under the load conditions, especially, the peak currents in the resonant inductor, the clamp diode and the clamp capacitor increase substantially. The simulated values of the peak current in the resonant inductor and clamp diode are very close to the calculated values using Equations 2.24 and 2.25. Simulation was also performed for a conventional hard switching inverter operated off the same DC source under the identical load conditions. It was found that the current stresses on the main devices are very similar in the hard switching and resonant inverter. The biggest penalty faced by the resonant inverter is obviously the elevated bus voltage; however, it can be limited using the active clamping.

3.3 Modeling with the Stray Inductance

A common problem in the conventional hard switching inverter is that the stray inductance leads to DC bus voltage overshoots, increased switching losses and reduced allowable switching frequency. In the resonant DC link inverter, the interconnection of the link components, widely separated due to physical dimensions, inherently increases the undesirable stray inductance. Moreover, the stray inductance effects may be amplified, as the operating frequency is very high in the resonant inverter.

Simulations were performed to investigate the operational behavior of the resonant link with non-ideal components. The simulated circuit is shown in Figure 3.6. The circuit model is based on an earlier implementation of an actively clamped resonant link. Modeled are the various stray inductance elements associated with the interconnections and equivalent series resistance (ESR) elements of the components.

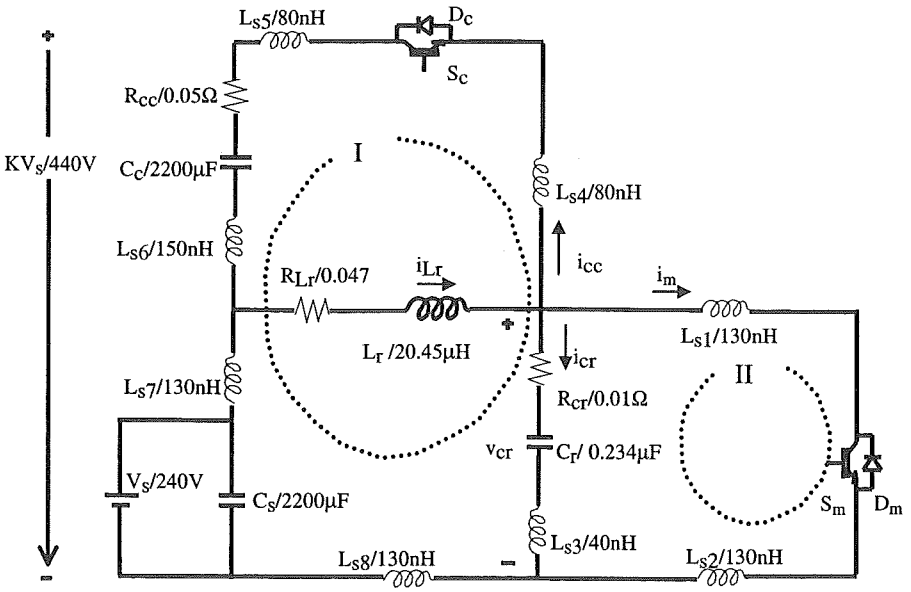


Figure 3.6. Simulation circuit for the actively clamped resonant DC link modeled with non-ideal components.

Figure 3.7 shows the simulated waveforms of the non-ideal resonant link operating under the same conditions as for the ideal case of Figure 3.2. The obvious difference between the simulated waveforms in Figure 3.7 and Figure 3.2 is that parasitic oscillations appear in the bus voltage waveform during the active clamping and the bus shorting. The oscillations during the active clamping increase the peak bus voltage to 477V, an overshoot of 37V above the clamping voltage, causing a performance degradation of the active clamping. The oscillations during the bus shorting deteriorate the zero voltage switching conditions for the inverter devices.

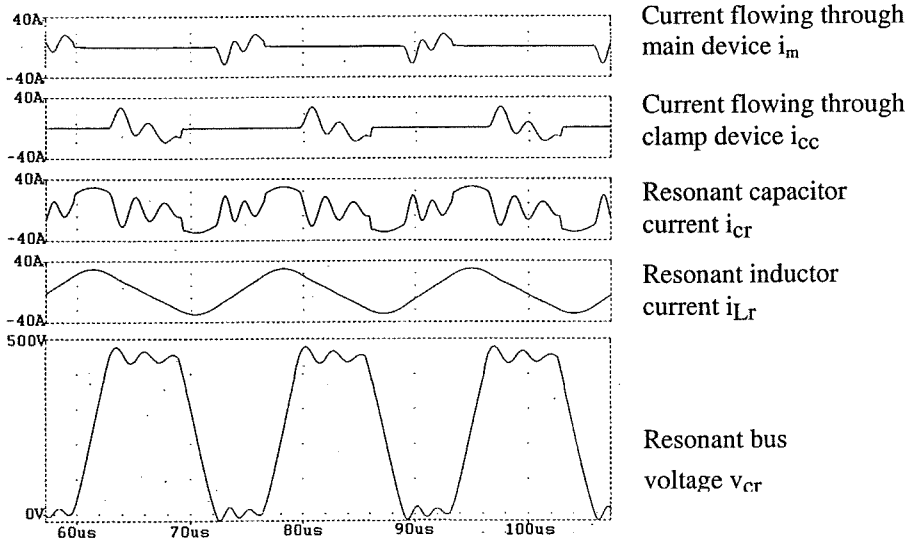


Figure 3.7. Simulated waveforms of the actively clamped resonant DC link with non-ideal components.

Circuit analysis shows that the parasitic oscillations during the active clamping and the bus shorting are caused by the interaction between the resonant capacitor and the stray inductances associated with the circuit loops I and II as shown in Figure 3.6, respectively. The peak overshoot above the clamping voltage can be found from Equation 3.1 [Skibinski, 1993b]

$$\Delta V_{overshoot}(I) = I_{ccp}\sqrt{\frac{\sum L_s(I)}{\sum C(I)}} \tag{3.1}$$

where

$$\sum L_s(I) = L_{s3} + L_{s4} + L_{s5} + L_{s6} + L_{s7} + L_{s8}$$
$$\sum C(I) = C_r // C_s // C_c \approx C_r$$

I_{ccp} is the peak current flowing through the clamp diode when it becomes forward biased, and I_{ccp} is given by Equation 2.17. $\sum L_s(I)$ is the sum of the stray inductances associated with the circuit loop I, and $\sum C(I)$ is the equivalent series capacitance in the circuit loop I. Equation 3.1 suggests that minimizing the stray inductance in loop I is the key to improving the performance of the active clamping. The oscillation frequency during the active clamping can be calculated from Equation 3.2. The calculated value of the oscillation frequency during the active clamping is 420kHz, and it is close to the one obtained from the simulation.

$$f_{osc}(I) = \frac{1}{2\pi\sqrt{\sum L_s(I) \cdot \sum C(I)}} \tag{3.2}$$

In circuit loop II, the peak overshoot above zero volts during the bus shorting can be found from Equation 3.3.

$$\Delta V_{overshoot}(II) = I_{Dm}\sqrt{\frac{\sum L_s(II)}{C_r}} \tag{3.3}$$

where

$$\sum L_s(II) = L_{s1} + L_{s2} + L_{s3}$$

I_{Dm} is the current flowing through the main diode, D_m, when the bus voltage reaches zero volts. For the resonant link under no load, this current is equal to the trip current, I_T, given by Equation 2.13. The parasitic oscillation frequency during the bus shorting is given by Equation 3.4.

$$f_{osc}(II) = \frac{1}{2\pi\sqrt{\sum L_s(II) \cdot C_r}} \tag{3.4}$$

The calculated value of the oscillation frequency during the bus shorting is 600kHz, and again it is close the simulated one.

From the simulations and analyses, it is found that the dominant stray inductances, which contribute the detrimental voltage oscillations, are associated with the following paths.

- From the resonant capacitor to the inverter stage and return (L_{s1}, L_{s2}, and L_{s3}).
- From the resonant capacitor to DC source, through the clamp device and clamp capacitor (L_{s4}, L_{s5}, and L_{s6}).
- From the DC source to the resonant link and return (L_{s7} and L_{s8}).

In other words, the positioning of the resonant inductor seems less important in terms of the effects of the stray inductances.

3.4 Summary

In this chapter, the operating principles and analyses of the actively clamped resonant DC link inverter have been verified. The capability of bidirectional power flow of the resonant inverter has been confirmed through the simulations. The inverter DC current prediction scheme has been shown to be an effective control technique to ensure reliable resonant operation. The simulation study shows that the additional current stresses on the main devices as a result of link resonance are minimal. The stray inductance in the resonant inverter may cause a higher peak bus voltage and non-zero voltage switching of the inverter devices. In the next chapter, a detailed analysis of power losses in the actively clamped resonant DC link inverter is presented.

CHAPTER 4

LOSS ESTIMATION

The motivation for the use of the resonant inverter stems from a desire to eliminate the switching losses in the inverter devices. This chapter presents a detailed analysis of the losses in the resonant DC link inverter. Equations for estimating the various losses in the resonant DC link inverter and an equivalent hard switching inverter are developed. Based on these equations, a design optimization is performed for the resonant DC link inverter to find the optimum values of the link components. Finally, a comparison of the losses in the resonant inverter and hard switching inverter is made.

4.1 Losses in the Hard Switching Inverter

In the hard switching inverter, the major power losses are the conduction and switching losses in the inverter devices. Conduction losses occur because the voltage drop across the device and the current flowing through the device occur simultaneously during conduction. Switching losses are incurred by the simultaneous presence of voltage and current on the device during switching. These losses can be calculated using simplified device models.

4.1.1 Conduction Losses

For conduction loss calculation, the device can be simplified as a constant voltage drop in series with a linear resistor. This simplified model is suitable for both IGBTs and diodes. The on-state voltages of an IGBT and a diode are expressed in Equations 4.1 and 4.2, respectively.

$$V_{ce} = V_q + I_q \cdot R_q \tag{4.1}$$

$$V_{ak} = V_d + I_d \cdot R_d \tag{4.2}$$

I_q and I_d are the currents flowing through the IGBT and diode, respectively. The parameters, V_q, R_q, V_d, and R_d can be extracted from data sheets. The power dissipated in a component with a constant voltage drop is the average current times the voltage drop. The power dissipated in a resistor is the rms current squared times the resistance. To simplify the calculation of the IGBT and diode currents, the load current is assumed to be sinusoidal. Given sinusoidal pulse width modulation, the average and rms currents of the IGBT and diode in a three-phase inverter can be calculated using Equations 4.3 to 4.6 [Berringer, 1995].

$$I_q(\text{avg}) = I_o(\text{pk})[\frac{1}{2\pi} + \frac{m_a \cos\phi}{8}] \tag{4.3}$$

$$I_q(\text{rms}) = I_o(\text{pk})\sqrt{\frac{1}{8} + \frac{m_a \cos\phi}{3\pi}} \tag{4.4}$$

$$I_d(\text{avg}) = I_o(\text{pk})[\frac{1}{2\pi} - \frac{m_a \cos\phi}{8}] \tag{4.5}$$

$$I_d(\text{rms}) = I_o(\text{pk})\sqrt{\frac{1}{8} - \frac{m_a \cos\phi}{3\pi}} \tag{4.6}$$

where $I_o(\text{pk})$ is the peak load current, ϕ is the power factor angle, and m_a is the modulation index. Using the simplified models, the conduction losses in the IGBT, $P_{q\text{-con}}$, and diode, $P_{d\text{-con}}$, are obtained using Equations 4.7 and 4.8.

$$P_{q-con} = V_q \cdot I_q(\text{avg}) + R_q \cdot I_q(\text{rms})^2 \tag{4.7}$$

$$P_{d-con} = V_d \cdot I_d(\text{avg}) + R_d \cdot I_d(\text{rms})^2 \tag{4.8}$$

The total conduction losses, $P_{tot\text{-con}}$, of six IGBTs and diodes are given by Equation 4.9.

$$P_{tot-con} = 6(P_{q-con} + P_{d-con}) \tag{4.9}$$

Clearly, given device characteristics, the conduction losses are only dependent on load conditions.

4.1.2 Switching Losses

In the hard switching inverter, three components of the switching losses can be identified; IGBT turn on losses, IGBT turn off losses, and the losses due to diode reverse recovery. The switching losses in the hard switching inverter can be calculated using the measured values of switching energy from the data sheets.

Data sheets normally give the measured values of turn-on and turn-off energy (E_{on} and E_{off}) for a typical test voltage and current (V_{test} and I_{test}). The measured values of turn-on energy include the losses due to diode reverse recovery [Siemens Data Book, 1995]. These values should be scaled appropriately for a specific application using Equation 4.10 [Clemente, 1995].

$$E_{tot} = K_g \cdot (E_{on} + E_{off}) \cdot \frac{V_S}{V_{test}} \cdot \frac{I_O(pk)}{I_{test}} \tag{4.10}$$

In Equation 4.10, V_S is the bus voltage, $I_O(pk)$ is the peak load current, and K_g is the correction factor to account for the gate drive impedance. The total switching losses, $P_{tot\text{-}sw}$, in the hard switching inverter can be calculated using Equation 4.11 [Berringer, 1995].

$$P_{tot-sw} = 6f_S \cdot \frac{E_{tot}}{\pi} \tag{4.11}$$

where f_S is the PWM switching frequency. The total losses given in Equation 4.12 in the hard switching inverter are the sum of the total conduction and switching losses.

$$P_{tot}(HSI) = P_{tot-con} + P_{tot-sw} \tag{4.12}$$

It is clear from Equation 4.11 that the switching losses in the hard switching inverter are directly related to the PWM switching frequency. Thus the achievable switching frequency is thermally limited due to the switching losses. Further, it can be seen from Equation 4.10 that switching energy is proportional to the voltage across the device during switching. Clearly, the switching losses can be eliminated if the voltage across the device is zero during the switching.

4.2 Soft Switching Losses

An important issue involved with the loss calculation for the resonant DC link inverter is to evaluate the switching losses in the device under zero voltage switching. The behavior of IGBTs under zero voltage switching differs significantly from that under hard switching conditions [Kurnia, 1995]. In the resonant inverter, the devices are turned on only when the antiparallel diodes are conducting; thus no dynamic saturation exists at device turn on. The higher peak voltage and current stresses resulting from diode recovery are also no longer relevant. The turn-on losses of device and the losses due to diode recovery are negligible, consequently, only the turn-off losses need to be considered [Divan, 1997].

If an IGBT carrying a current I_Q is switched off in a zero voltage switching circuit as shown in Figure 4.1, the difference between I_Q and the instantaneous device current flows into a resonant capacitor, C_r, connected directly in parallel to the device. This current determines the voltage waveform. An IGBT turn-off waveform for such a case is illustrated in Figure 4.2a. The turn-off current of the IGBT is characterized by a sharp decrease in current, taking only about 50ns for a 50A/600V IGBT. This is a result of the MOSFET part of the IGBT turning off. The bipolar part is still conducting, but the carriers are swept away quickly by tail current. The complete fall time, t_f, is about 550ns for the 50A/600V IGBT.

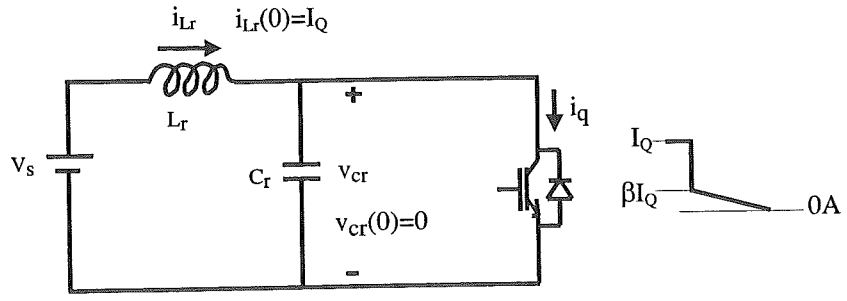


Figure 4.1. A zero voltage switching circuit for characterising IGBT turn-off behaviour.

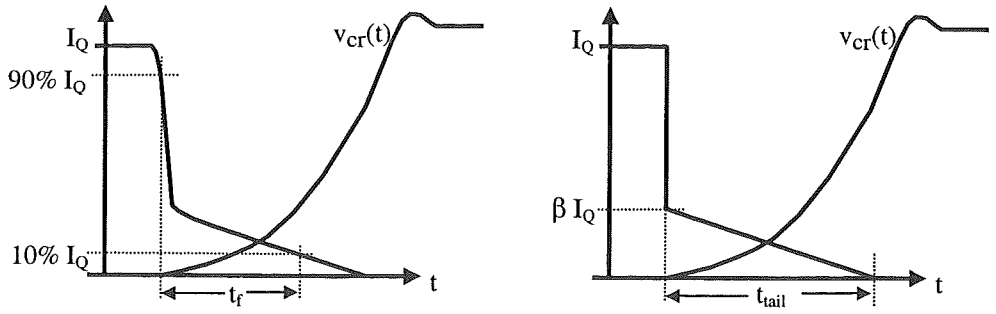


Figure 4.2. (a) Realistic IGBT turn-off waveforms under zero voltage switching. (b) Idealized model for calculation of soft switching losses.

A simplified model of this switching behavior is shown in Figure 4.2b. β defines a break point of the IGBT current waveform. The value of β is about 0.25 to 0.3 obtained from the extensive experimental tests of IGBTs under the zero voltage switching conditions [Kurnia, 1995]. The time t_{tail} is considered to be the end of the current flow rather than the fall time, t_f, where the current is still 10% of I_Q. Under these assumptions, the initial current in the resonant capacitor is $(1-\beta)\ I_Q$, and the IGBT current decreases linearly from βI_Q to zero taking the time of t_{tail}. The differential equations 4.13 and 4.14 govern the circuit behavior after the IGBT is switched off.

$$i_{Lr} = C_r \frac{dv_{cr}}{dt} + \frac{\beta I_Q}{t_{tail}}(t_{tail} - t) \tag{4.13}$$

$$L_r \frac{di_{Lr}}{dt} = V_s - v_{cr} \tag{4.14}$$

Solving Equations 4.13 and 4.14 with the initial conditions, $i_{Lr}(0) = I_Q$ and $v_{cr}(0) = 0$, the expression for the bus voltage with the impact of the tail current taken into account is found and given in Equation 4.15.

$$v_{cr}(t) = (1-\beta)I_Q Z_r \sin\omega t + (1-\cos\omega t)\left(V_S + \frac{\beta I_Q L_r}{t_{tail}}\right) \tag{4.15}$$

Multiplying this voltage with the device current and integrating up to t_{tail} yields an expression for the turn-off energy for the IGBT carrying the current I_Q as given in Equation 4.16 [Mertens, 1990].

$$E_{off}(I_Q) = Z_r I_Q{}^2 \beta(1-\beta)\left(\frac{1}{\omega} - \frac{\sin \omega t_{tail}}{\omega^2 t_{tail}}\right) + \left(V_S \beta I_Q + \frac{\beta^2 I_Q{}^2 L_r}{t_{tail}}\right)\left[\frac{t_{tail}}{2} - \frac{(1-\cos \omega t_{tail})}{\omega^2 t_{tail}}\right] \quad (4.16)$$

It is noticed from Equation 4.15 the rate of the increase of the bus voltage is mainly governed by the resonant impedance, therefore, the turn-off energy given in Equation 4.16 is directly related to the resonant impedance. At a specified resonant frequency, a smaller value of the resonant impedance indicates a larger value of the resonant capacitance, and gives a slower rise of the bus voltage when the tail current still persists and results in lower turn-off losses. With turn-off energy calculated, switching losses can then be found by multiplying turn-off energy with the switching frequency.

4.3 Losses in the Resonant Inverter

The total losses in the resonant inverter are made up of conduction and switching losses in the seven devices and losses in the ESRs of the resonant link. These losses are individually calculated.

4.3.1 Main Device Conduction Loss

Since the main devices are minimally involved with the link resonance, the conduction losses in the main IGBTs (S_1-S_6) and diodes (D_1-D_6) are almost independent of the link components. The resonant inverter modulated by the synchronized PWM behaves almost exactly like the hard switching PWM inverter

operated off the same supply voltage, it is characterized by the same output voltage to the supply voltage ratio. Thus, under the same load conditions and for the same devices, the conduction losses of main IGBTs and diodes in the resonant inverter, $P_{main\text{-}con}$, are almost the same as in the hard switching inverter given by Equation 4.9 and are re-expressed as Equation 4.17.

$$P_{main-con} = 6(P_{q-con} + P_{d-con}) \tag{4.17}$$

4.3.2 Main Device Switching Loss

The switching losses in the main devices depend primarily on the resonant capacitor and indirectly on the resonant inductor. As explained in Section 4.2, only turn-off switching losses need to be considered. When the peak load current, $I_o(pk)$, is turned off in a main device, the resulting turn-off energy, $E_{off}[I_o(pk)]$, can be calculated using Equation 4.16 with I_Q replaced by $I_o(pk)$. In the resonant inverter, the switching frequency of the main devices varies and depends mainly on the resonant frequency f_r. The highest switching frequency occurs whenever the output voltage is zero volts, and equals the resonant frequency. The average switching frequency of the main devices equals half the resonant frequency [Divan, 1993]. The switching losses in the six main devices, $P_{main\text{-}sw}$, can be found using Equation 4.18.

$$P_{main-sw} = 6\frac{f_r}{2}E_{off}[I_o(pk)] \tag{4.18}$$

4.3.3 Clamp Device Conduction Loss

When the resonant inverter is under load, the current flowing through the clamp device increases whenever the inverter DC current decreases. This incurs additional losses in the clamp device, which are load-dependent and difficult to estimate. For the loss calculation, it is assumed that the losses in the clamp IGBT and diode are independent of the inverter DC current and can be calculated for the resonant

inverter under no-load conditions. The average and rms currents in the clamp IGBT and diode are found using Equations 4.19 and 4.20.

$$I_{clamp-q}(avg) = I_{clamp-d}(avg) = I_{ccp} \cdot t_c \cdot \frac{f_r}{2} \tag{4.19}$$

$$I_{clamp-q}(rms) = I_{clamp-d}(rms) = \sqrt{f_r \frac{(K-1)^2 V_s{}^2 t_c{}^3}{3L_r{}^2}} \tag{4.20}$$

where I_{ccp} is the peak current flowing through the clamp device and is given by Equation 2.17, and t_c is the conduction time of the clamp device and is given by Equation 2.18. The total conduction losses in the clamp IGBT and diode, $P_{clamp\text{-}con}$, can then be calculated using the simplified models and are given by Equation 4.21.

$$\begin{aligned} P_{clamp-con} = {} & V_q \cdot I_{clamp-q}(avg) + R_q \cdot I_{clamp-q}(rms)^2 \\ & + V_d \cdot I_{clamp-d}(avg) + R_d \cdot I_{clamp-d}(rms)^2 \end{aligned} \tag{4.21}$$

4.3.4 Clamp Device Switching Loss

The clamp IGBT is also switched under zero voltage switching conditions. Equation 4.16 for the calculation of turn-off energy holds true for the clamp IGBT. The peak current to be switched off in the clamp IGBT is I_{ccp} given by Equation 2.17. The turn-off energy of the clamp IGBT, $E_{off}(I_{ccp})$, can then be calculated using Equation 4.16 with V_S replaced by $(K-1)V_S$ and I_Q replaced by I_{ccp}. The clamp IGBT operates at the resonant frequency. The switching loss in the clamp device is determined by Equation 4.22.

$$P_{clamp-sw} = f_r \cdot E_{off}(I_{ccp}) \tag{4.22}$$

4.3.5 ESR Losses

As the current circulates in the resonant link, losses are incurred in ESR elements. The ESR losses in the resonant capacitor can be neglected since the resonant capacitor has a very high quality factor. Also, the ESR losses in the clamp capacitor can be ignored because the rms current in the clamp capacitor is very low. Therefore, only the ESR losses in the resonant inductor need to be considered.

When the resonant inverter operates with a load, the inductor current oscillates following the changes of the inverter DC current. The inductor current waveform is quite complex, and it is difficult to derive a closed form expression for the rms current. For an approximate calculation, the inductor current can be assumed to have two independent components, the inverter DC current and the AC resonant current. The average inverter DC current is load-dependent and given by Equation 4.23 [Mohan, 1995].

$$I_X(\text{avg}) = \frac{3}{4} m_a I_O(\text{pk}) \cos\phi \tag{4.23}$$

The rms resonant current, I_{Lr}(rms), is given by Equation 2.22. The ESR value of the resonant inductor is determined by the inductor quality factor Q. The losses in the resonant inductor, P_{Lr}, are then obtained using Equation 4.24.

$$P_{Lr} = \frac{Z_r}{Q} I_X(\text{avg})^2 + \frac{Z_r}{Q} I_{Lr}(\text{rms})^2 \tag{4.24}$$

The total losses in the actively clamped resonant DC link inverter can now be calculated by summing the main devices losses, the clamp device losses and the resonant inductor losses, and are given in Equation 4.25.

$$\begin{aligned} P_{tot}(\text{ACRLI}) = {} & P_{main-con} + P_{main-sw} + P_{clamp-con} \\ & + P_{clamp-sw} + P_{Lr} \end{aligned} \tag{4.25}$$

4.4 System Optimization

The design of the resonant DC link inverter commences with the selection of the switching devices. Given the device characteristics, the resonant components L_T and C_r can then be chosen to minimize the total losses.

Six-pack 50A/600V IGBT modules (BSM50GD60DN2, Siemens) are selected as the main devices of the inverter stage and the clamp device of the resonant link. Data sheets for this IGBT module are included in Appendix C. A clamping ratio of 1.83 is used to give a clamping voltage of 440V and constrain the bus voltage below 500V. Design considerations for the selection of the switching devices and the clamping ratio are further detailed in Section 5.1.4.

The resonant frequency is usually specified for the required spectral performance. The maximum resonant frequency achievable in the real circuit is limited by several factors including device switching characteristics, thermal constraints from the clamp device, and availability of the passive components [Schulting, 1992]. For the prototype resonant DC link inverter, a synchronized PWM scheme is used to modulate the inverter. In this scheme the sinusoidal PWM signals are sampled at the resonant frequency and then synchronized to the zero crossing of the bus voltage. Simulations show that a resonant frequency of about 5 times of the PWM switching frequency is adequate to preserve the well-defined switching pattern of the sinusoidal PWM signals. For a maximum PWM switching frequency of 14kHz considered, a resonant frequency of 70kHz is chosen for the design of the link components. Given the resonant frequency, the values of the resonant components can be determined if the resonant impedance is known.

For the resonant link under no load, the losses in the resonant link are governed by the resonant current, which is approximately determined by V_S/Z_T. A larger value of the resonant impedance results in a lower current in the resonant link and lower losses. With the resonant inverter under load, the load-dependent DC current flows through the resonant inductor. A larger value of the resonant impedance suggests a larger

value of resonant inductance, and this in turn causes more ESR losses in the inductor since more turns are required to build the inductor. For the inverter stage, on the other hand, a small value of the resonant impedance is desirable to make the bus voltage increase slowly when the inverter devices are switched off. Clearly, an optimum value of the resonant impedance exists, which gives the lowest losses in the resonant DC link inverter.

Based on the equations derived in the previous sections, a computer program has been developed to calculate the total losses in the resonant inverter and hard switching inverter. This program is listed in Appendix B. Figure 4.3 shows design optimization curves for the resonant DC link inverter using IGBTs operated off the supply voltage of 240V. For loss calculations, the load is assumed to be a sinusoidal current source of 25A rms with a power factor of 0.86 and a modulation index of 0.62. These load conditions are similar to those expected for the electric vehicle application. A clamping ratio of 1.83 and a realistic inductor quality factor of 190 are used for the loss calculations. The model parameters, V_q=0.85V and R_q=0.017Ω, are used to calculate the conduction losses of the IGBTs. The model parameters, V_d=1.04V and R_d=0.012Ω, are used to calculate the conduction losses of the diodes. The values, β=0.3 and t_{tail}=800ns, are used to calculate the soft switching losses. Loss calculations are performed for the different values of the resonant impedance while the resonant frequency is constant at 70kHz.

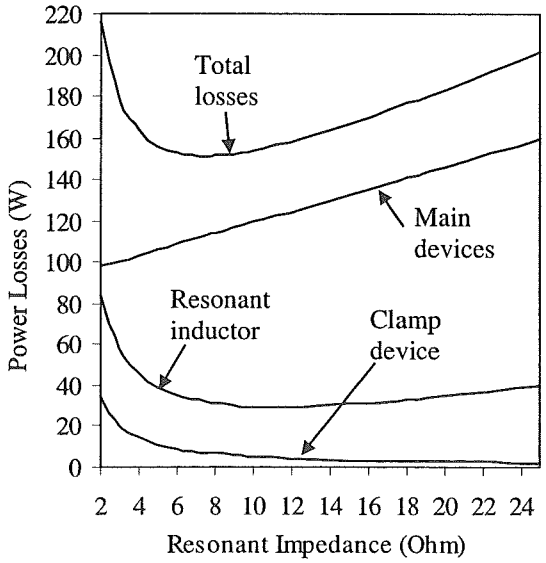


Figure 4.3. Variation of the losses in the ACRLI due to the resonant impedance.

It is observed from Figure 4.3 that with a decrease in the resonant impedance the losses in the main devices decrease, whereas the losses in the resonant inductor and in the clamp device increase. In particular, the losses in the resonant inductor and clamp device increase dramatically for the impedance values below 6Ω. The load-dependent losses in the ESR of the inductor seem to be insignificant given a high quality factor, as can be seen there is only a small increase of the losses in the inductor while the value of the resonant impedance is increased. Examining the curve of the total losses, the tradeoff between the link losses and the main devices' switching losses is clearly exhibited. The total losses in the resonant DC link inverter are very sensitive to the resonant impedance. For the values of the resonant impedance considered, the total losses in the resonant inverter have a maximum variation of 43% above the lowest loss value.

For the given application, the optimum value of the resonant impedance is around 8.5Ω. Given the resonant frequency of 70kHz this value of the resonant impedance corresponds to a resonant inductance of 19.2μH and a resonant capacitance of 0.267μF. In practice the required resonant capacitance is obtained by paralleling several small capacitors, therefore only the discrete values of the resonant capacitance can be obtained. For the final implementation of the prototype resonant DC link inverter, the closest values of resonant inductance of 20.45μH and resonant capacitance of 0.234μF are used. This combination gives a value of resonant impedance of 9.35Ω and a natural resonant frequency of 72.7kHz.

Using the impedance value of 9.35Ω, the various losses in the resonant inverter are re-evaluated. For a comparison, the losses in the hard switching inverter using the same IGBTs under the identical operating conditions are also calculated. The model parameters for the calculations of the conduction losses in the hard switching inverter are the same as those used for the resonant inverter. For the calculations of the switching losses in the hard switching inverter, the model parameters, E_{on}=2.3mWs, E_{off}=5.0mWs (for V_{test}=300V, I_{test}=50A), and a gate drive correction factor K_g of 1.2, are used. The calculated results are summarized in Table 4.1.

Table 4.1 Calculated Losses in the HSI and ACRLI

	Frequency (kHz)	Main Devices (W)		Resonant Link (W)		Total Losses (W)
		Conduction	Switching	Inductor	Clamp Device	
HSI	4	90	38			128
	14	90	133			223
ACRLI	70	90	27	30	6	153

It can be seen from Table 4.1 that for the resonant inverter the switching losses in the main devices are substantially reduced, and the conduction losses in the main devices are the major loss component. Under the identical load conditions, the resonant inverter has an 80% reduction in the main devices' switching losses by compared with the hard switching inverter operating at a PWM switching frequency of 14kHz. Including the link losses, the resonant inverter still has a 30% reduction in the total power losses. The lower switching losses allow the resonant inverter to operate at a substantially higher switching frequency, and have a strong potential for realizing higher performance and power density. For the hard switching inverter, on the other hand, switching losses completely dominate the total losses at a high switching frequency of 14kHz and limit any further increase of the switching frequency. At a low PWM switching frequency of 4kHz the hard switching inverter is more efficient, where the switching losses are very low and the conduction losses are dominant.

4.5 Summary

This chapter has presented a detailed analysis of the losses in the resonant DC link inverter. The analysis shows that with the decrease of the resonant impedance the losses in the main devices decrease, whereas the losses in the resonant link increase. Using the overall losses as a criteria, the design optimization for the resonant DC link inverter intended for the electric vehicle application yields an optimal value of the resonant impedance as 8.5Ω. However due to the limitation of the resonant capacitors the closest impedance value of 9.35Ω is determined for the implementation of the prototype resonant DC link inverter. This impedance value corresponds to a combination of a resonant inductance of 20.45μH and a resonant capacitance of

0.234μF. Loss calculations show that in the resonant inverter the switching losses in the main devices are substantially reduced, and the conduction losses become the major loss component. Under the identical expected load conditions the resonant inverter has an 80% reduction of the switching losses in the main devices and a 30% reduction of the total losses in comparison to the hard switching inverter operating at a PWM switching frequency of 14kHz. In the next chapter the construction of the prototype resonant DC link inverter is detailed.

CHAPTER 5

CONSTRUCTION

This chapter presents the design and selection of the components used to implement the prototype resonant DC link inverter. The construction of the prototype resonant inverter is detailed to show how the stray inductance in the constructed resonant inverter is minimized.

5.1 Components

The components needed to realize a resonant DC link inverter include the resonant inductor, resonant capacitor, clamp capacitor, and switching devices for the inverter stage and the active clamping. The design and selection of these components are described in this section.

5.1.1 Resonant Inductor

The resonant inductor carries the inverter DC current and the resonant current. The average value of the inverter DC current is dependent on the load conditions, whereas the resonant current is dependent on the resonant link parameters and has a resonant frequency of about 70kHz. Further, the amplitude of the resonant current is even larger than the average value of the inverter DC current. Thus ferrite cores are suitable for the resonant inverter application due to low core losses at a high operating frequency.

A large pot core ferrite (PM114/93, ferrite N27, Siemens) was readily available for use in this project. The data sheets for this set of pot cores are included in Appendix C. The power handling capability of this ferrite core is assessed against the required

specifications using Equation 5.1 [Undeland, 1996].

$$L_r I_{Lr}(rms) I_{Lr}(pk) = K_{cu} A_w A_c J_{rms} B_{pk} \quad (5.1)$$

The quantities on the left side of Equation 5.1 are the required specifications, L_r is the required resonant inductance, 20.45μH, determined by the design optimization in Section 4.4, $I_{Lr}(rms)$ and $I_{Lr}(pk)$ are the rms and peak currents in the resonant inductor under the rated load conditions, respectively. According to the simulation results (Table 3.1 in Section 3.2), $I_{Lr}(rms)$ is 25.4A rms and $I_{Lr}(pk)$ is 62A. On the right side of Equation 5.1, K_{cu} is the copper fill factor and can be assumed to be 0.3 for Litz wire. A_w is the area of the winding window of the core, and A_c is the cross-sectional area of the core, these two quantities can be obtained from the data sheets of the core, and A_w is 1399 mm^2 and A_c is 1720mm^2. J_{rms} is the rms current density in the inductor winding, and B_{pk} is the peak flux density in the core, these two quantities can be calculated by evaluating the thermal model of the inductor. To assess the core capability it is assumed that the power dissipated in the inductor is uniformly distributed in the copper winding and the magnetic core, and that the maximum allowable surface temperature of the inductor is 100°C and the ambient temperature is 40°C [Undeland, 1996]. Under these assumptions the quantities J_{rms} and B_{pk} are calculated, and J_{rms} is 2.78A/mm^2 and B_{pk} is 155mT. The product on the right side of Equation 5.1, $K_{cu}A_wA_cJ_{rms}B_{pk}$, is then calculated to be 0.1445 H-A^2, whereas the product, $L_rI_{Lr}(rms)I_{Lr}(pk)$, is calculated to be 0.0322 H-A^2. Clearly, this ferrite core has a large enough power capability to meet the required specifications, but it is not an optimal core for this application.

The inductor winding was wound with two Litz wires, evenly twisted together, to give a low DC resistance. These Litz wires were used because they were already available from a previous project. Each Litz wire has a length of 97cm, thus a maximum of 5 turns can be wound round the given bobbin. For the required inductance of 20.45μH and the limited 5 turns, the peak flux density, B_{pk}, needs to be adjusted to

the value given by Equation 5.2 [Mohan, 1995].

$$B_{pk} = \frac{L_r I_{Lr}(pk)}{NA_c} \tag{5.2}$$

In Equation 5.2, L_r is the required inductance, $I_{Lr}(pk)$ is the peak inductor current, N is the number of turns of the inductor winding, and A_c is the cross-sectional area of the core. Using Equation 5.2, B_{pk} is calculated to be 147mT. This value is still lower than that calculated from the thermal model. Therefore 5 turns of winding seem to be acceptable although more turns are desirable to reduce the peak flux density and core losses.

The air gap length, l_g, is then tailored to give the peak flux density of 147mT when the peak inductor current is 62A. Under assumption that the magnetic reluctance is only caused by the air gap, the required air gap length of 2.6mm are calculated using Equation 5.3 [McLyman, 1988].

$$l_g = \frac{4\pi \cdot 10^{-7} \cdot N \cdot I_{Lr}(pk)}{B_{pk}} \tag{5.3}$$

The another important purpose of introducing the air gap is to prevent core saturation. The impedance of the resonant inductor in the saturation region may fall to a value close to the DC winding resistance, and this low resistance may allow a damagingly high current to flow through the inverter devices during the bus shorting. In the electric vehicle the motor current of up to 75A rms can be expected when the maximum acceleration is required [Williams M., 1993]. Under this transient load condition, the peak inductor current can be estimated as high as 132A, and the peak flux density of 314mT is calculated using Equation 5.3. The saturation flux density for the given core material (N27) is 510mT [Siemens Data Book, 1991]. Therefore the designed resonant inductor has a sufficient margin of the flux density in the core to cope with the peak current of 132A without causing core saturation.

At an operating frequency of 70kHz and a peak flux density of 147mT, the specific power dissipated in the core is about 60mW/cm^3 for the ferrite material N27 [Siemens Data Book, 1991]. The total core losses of about 21W are then estimated for the

whole core volume. On the other hand, considering the winding losses, the total copper area of the inductor winding with two Litz wires paralleled is about 20.67mm^2, and the calculated DC resistance of the winding is only about 1.03mΩ. For the AC resistance of the winding, the consequence of the skin effect can be assumed to be neglected as the diameter of each strand of Litz wire is 0.29mm, which is less than twice the skin depth of 0.283mm at 70kHz [Mohan, 1995]. For a coarse estimation, the AC resistance can be considered as large as 10 times the DC resistance due to the proximity effect [Mohan, 1995]. Therefore the winding losses of about 6.6W are estimated, and the total losses in the inductor including core losses and winding losses are 27.6W with the inductor current of 25.4A rms, giving the equivalent series resistance of 42mΩ.

By separating two core halves with the proper thickness of plastic shims, the required air gap length of 2.6mm was obtained. In practice, to avoid the eddy losses that may be caused by the fringing flux across the air gap, any metal objects (like bolts) required for mechanical assembly of the resonant inductor should not be located in the vicinity of the air gap.

5.1.2 Resonant Capacitor

Metallized polypropylene capacitors are commonly used as the IGBT snubber capacitors in the power electronic field. The advantages include low loss, high current ratings, high reliability, small size and low cost [Williams N., 1996]. In the resonant DC link inverter, the resonant capacitor can also be regarded as a snubber, which is periodically reset by resonating with the resonant inductor [Mertens, 1990].

Polypropylene film capacitors (MKP10 Series, WIMA) were chosen to constitute the resonant capacitor in the prototype resonant inverter mainly due to low dielectric loss. Each selected film capacitor has a rated capacitance value of 0.047μF and a rated working voltage of 1000V DC. The required resonant capacitance of 0.234μF was obtained by connecting five these capacitors in parallel. Based on the simulation results of the resonant inverter under the rated load conditions (Table 3.1 in Section

3.2), the rms current of 3.8A is estimated for each film capacitor, and this current would not cause excessive losses to overheat the capacitor [Williams N., 1996].

5.1.3 Clamp Capacitor

The purpose of using the active clamping is to temporarily store the energy extracted from the resonant tank, with the net charge transferred to the clamp capacitor being zero over a few resonant cycles. The value of the clamp capacitance needs to be chosen to allow only a small variation in the clamping voltage

The methods for sizing the clamp capacitance are not available in the published literature. In this section an attempt is made to size the capacitance by assuming that the peak load current of 35A (25A rms) reverses and flows back to the resonant link. Under this condition the peak current of 72A in the clamp diode is estimated using Equation 2.25, and the diode conduction time of 7.37μs is calculated using Equation 2.26. The charge transferred to the clamp capacitor with the clamp diode conducting is then 265×10^{-6}C. Knowing the charge imposed on the clamp capacitor, the required capacitance can be calculated given an allowable rise in the clamping voltage. For instance, a capacitance value of 265μF gives a rise of only 1V in the clamping voltage ignoring the voltage overshoot caused by the stray inductance. For the prototype resonant inverter, a sufficiently large capacitance value of 2200μF was used to produce a virtually constant clamping voltage. The clamp capacitor consists of two electrolytic capacitors connected in parallel, and each of them has a rated capacitance of 1100μF and working voltage of 350V DC.

5.1.4 Switching Devices

There are two induction motors installed in the electric vehicle and each drive one rear wheel separately. Each induction motor has a nominal rated power of 2.2kW. The current ratings of the switching devices in the prototype resonant inverter were determined based on such an arrangement in which one resonant inverter is dedicated to one of the induction motors, allowing a torque controller to be used to control each induction motor. Line current drawn by one induction motor is about 25A rms at

rated torque and up to 75A rms at peak torque [Williams M., 1993]. Thus the selected switching devices should be able to handle a peak current of 106A.

It is highly desirable that the 600V devices can be used as the switching devices for the resonant inverter, as a 600V device has a lower saturation voltage, therefore lower conduction losses compared to a 1200V device. In the electric vehicle the DC supply voltage can vary from 180V to 280V depending the charge state of the batteries. As discussed in Section 2.2.1, the use of the active clamping allows the resonant bus voltage to be limited to an acceptable level. For the prototype resonant inverter, a clamping ratio of 1.83 was chosen to give a clamping voltage of 440V at the nominal supply voltage of 240V. The peak bus voltage is expected to be constrained below 500V even with a large voltage overshoot caused by the stray inductance (refer to Figure 3.7). This gives an adequate margin for 600V devices. At the maximum supply voltage of 280V, the clamping ratio may need to be adjusted to a lower value.

From the above considerations of current and voltage ratings, six-pack 50A/600V IGBT modules (BSM50GD60DN2, Siemens) including fast free-wheel diodes were selected as the switching devices of the resonant inverter. The data sheets for these IGBT modules are given in Appendix C. In order to handle the peak load current of 106A at peak torque the top and bottom three IGBTs in each module are connected in parallel to obtain a current rating of 150A. Further, The loss calculation (Table 4.1 in Section 4.4) has shown that the switching losses in the resonant inverter are substantially reduced and the power losses in the inverter devices are mainly the conduction losses. Therefore, the selected IGBT module has an adequate current margin to handle the peak load current.

One module is used to form one phase leg of the resonant inverter, and three modules are required to realize the inverter stage. Figure 5.1 shows one leg of the inverter stage. The collectors of the top three IGBTs, i.e., the pin P+ of the module, are connected to a positive bus, and the emitters of bottom three IGBTs, i.e., the pin N- of the module, are connected to a negative bus. The output pins, U, V and W, are linked together forming one phase output. The gates of the three paralleled IGBTs in each group are tied together and driven by a single gate signal. Gate drive printed circuit boards (PCBs) were available from a previous IGBT inverter project [Li, 1999]. Each

gate drive PCB consists of two identical gate drive circuits, one drive for the top three IGBTs and the another for the bottom three IGBTs. The gate drive was designed to have a peak gate current of up to 2A and two-stage short circuit protection [Li, 1999].

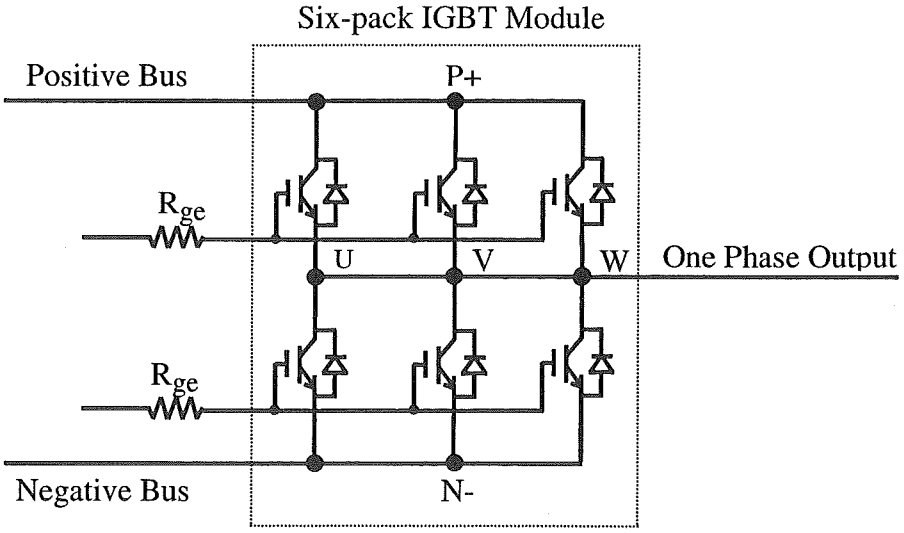


Figure 5.1. One leg of the resonant inverter using the six-pack IGBT module.

Similarly, the top three IGBTs in one selected module are paralleled, and used as the clamp device. Table 5.1 gives a summary of the components used to implement the prototype resonant DC link inverter.

Table 5.1 Components for the Prototype Resonant DC Link Inverter

Inverter devices	50A/600V IGBT module per phase leg
Clamp device	50A/600V IGBT module
Resonant inductor	20.45μH, core PM114/93 N27, 5 turns Litz wire, air gap 2.6mm
Resonant capacitor	0.234μF, 5×0.047μF 1000VDC polypropylene capacitors in parallel
Clamp capacitor	2200μF, 2×1100μF 350VDC electrolytic capacitors in parallel

5.2 Construction

The component layout of the prototype resonant DC link inverter is shown in Figure 5.2. The IGBT module, used as the clamp device, was mounted together with the IGBT modules for the inverter legs on a common large heatsink. In this way, the clamp device can be connected to a laminated bus (to be described shortly) with a short distance. All the IGBT modules were placed with the gate pin side outward and the power pin side inward, allowing wide copper bars can be run and connected to the power pins. A slot was created in the heatsink to accommodate the five film capacitors, which form the resonant capacitor. These film capacitors were placed with the pins upward and would be soldered to the laminated bus bars. Two 1100μF/350V DC electrolytic capacitors connected in parallel, referred as the supply capacitors, were included to the inverter system to essentially offset the stray inductance of the long cables from the resonant inverter to the battery bank. The clamp capacitors were located in a place as close as possible to the supply capacitors and the clamp device to minimize the interconnection distance.

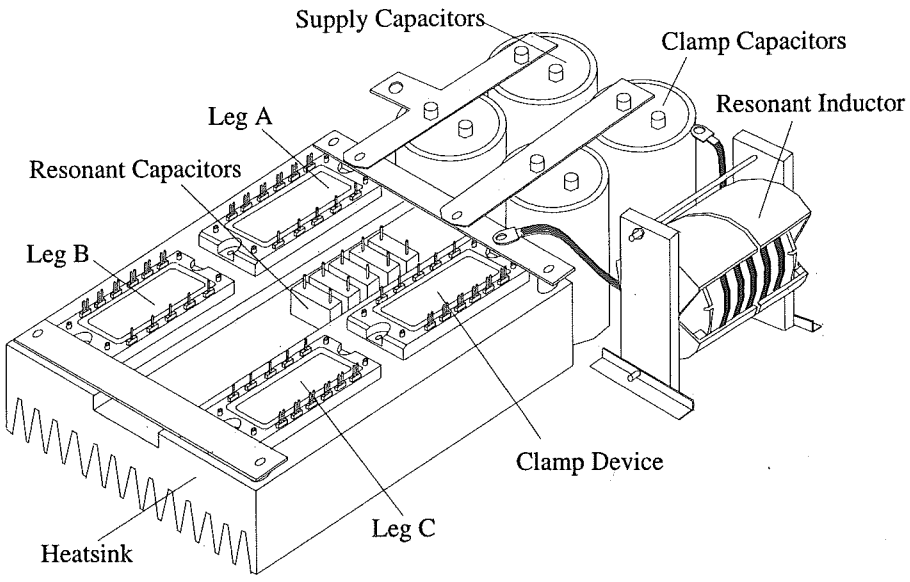


Figure 5.2. Physical layout of the components.

The connections in the bottom layer are shown in Figure 5.3. Three rectangular copper bars were used to connect three phase legs to an output terminal bar, from this terminal bar the connections from the resonant inverter to the induction motor can be made. Using a ' L ' shaped copper bar, the collector of the clamp device, i.e., the pin P+ of the IGBT module, was connected to the positive terminals of the clamp capacitors. The linking between the clamp capacitors and the supply capacitors were made using a flat copper plate, which was placed on an insulating board.

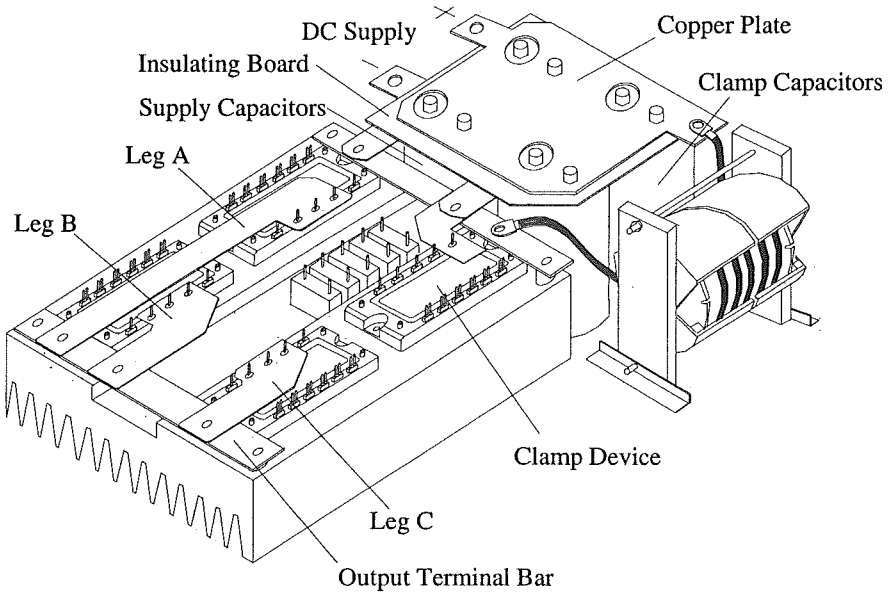


Figure 5.3. Bottom layer for the output connections.

With the connections on the bottom layer completed, an insulating board was then placed above the bottom layer as shown in Figure 5.4. This insulating board has a rectangular window, through this window the five film capacitors can be soldered to the laminated bus, which was placed above this insulating board and composed of two copper plates and a insulating layer sandwiched-in between two copper plates.

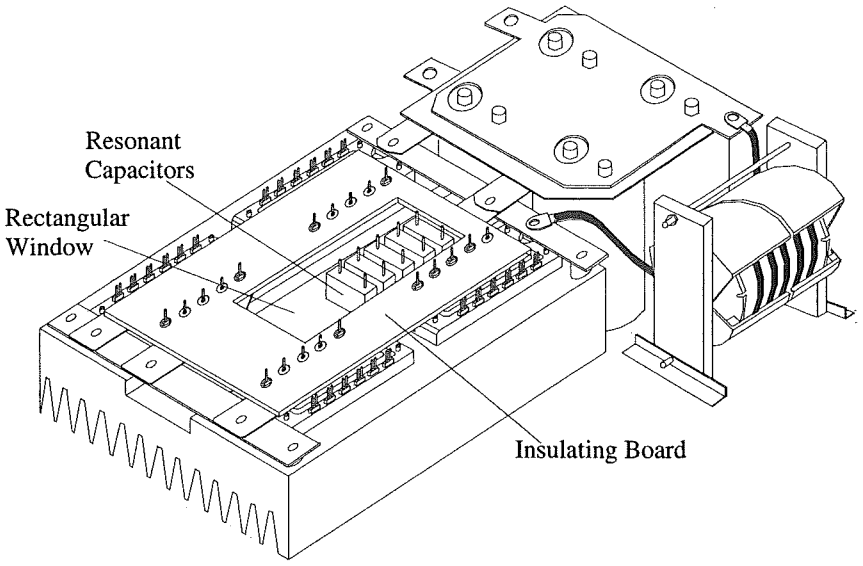


Figure 5.4. Insulating board between the bottom layer and the laminated bus.

From Figure 5.5, a copper plate, the positive bus bar of the laminated bus, can be seen to provide linking between the resonant inductor and the IGBT modules. The pin P+ of each leg module and the pins U, V and W of the clamp module were soldered to the top of the positive bus bar. One pin of each film capacitor was also soldered to the top of this bus bar. The other component pins were insulated with a proper length of heat-shrink tubes and isolated from the positive bus bar through the big holes.

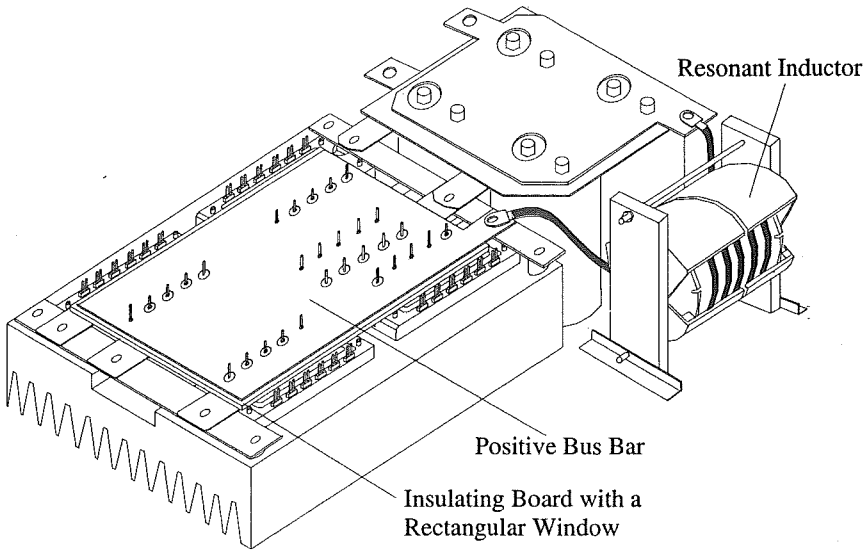


Figure 5.5. Positive bus bar of the laminated bus.

Stacked above the positive bus bar are the insulating layer and then the negative bus bar of the laminated bus. From Figure 5.6, a copper plate, the negative bus bar of the laminated bus, can be seen to provide the linking between the return terminal of the DC supply and the IGBT modules. The pin N- of each leg module was soldered to the negative bus bar. With one pin of each film capacitor soldered to the positive bus bar, the second pin of each film capacitor was soldered to this negative bus bar.

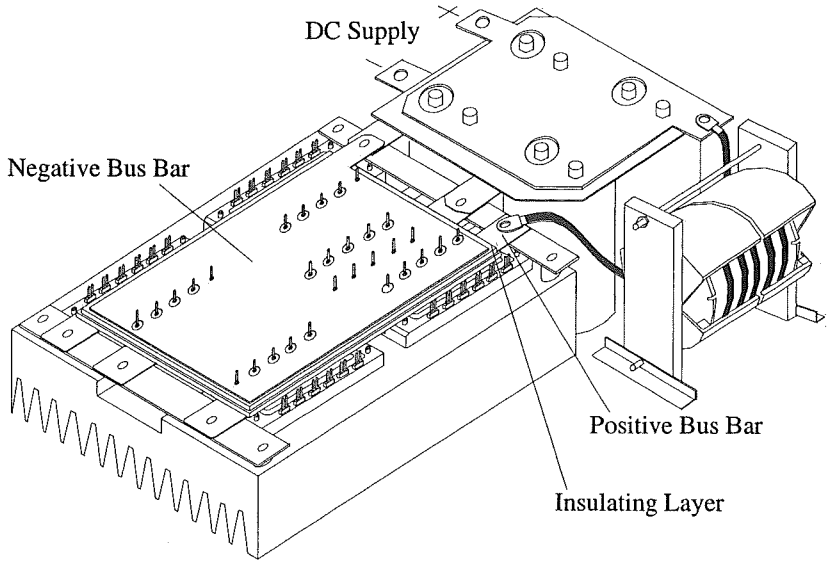


Figure 5.6. Laminated bus.

The inductance per unit length of a wide bus bar is about 1/2 to 1/3 that of a round conductor with the same cross-sectional area [Skibibski, 1993a]. Using a laminated bus structure, with two bus bars spaced close together and with an opposite current flow, the inductance per unit length of each bus bar can be further reduced, since the wide bus bars maximize the subtractive mutual inductance by canceling the mutual flux [Skibinski, 1993a]. Theoretical calculation shows that the inductance of the laminated bus bar for this assembly is only 9nH for the full length at the operating frequency of 70kHz.

It is expected that the stray inductances associated with the circuit from the resonant capacitor to the inverter stage and return (loop II as shown in Figure 3.6 in Section 3.3) were reduced greatly by using the laminated bus structure and embedding the resonant film capacitors into the laminated bus. The stray inductances associated with

the clamping path (loop I as shown in Figure 3.6 in Section 3.3) were also minimized by minimizing the interconnection distances and using the copper bars for the connections of the components.

After the connections for power circuit completed, the next step was then to connect the gate drive signals. From Figure 5.7 it can be seen that four interface printed circuit boards were soldered directly to the IGBT modules. These PCBs provide the parallel connection of the gate terminals of the three paralleled IGBTs in one module. On the PCB the collector, gate and emitter of each IGBT group are connected to the plugs, from these plugs, the connections to the gate drive board can be made. The collector signal is required to detect the de-saturation for the two-stage protection of the IGBT.

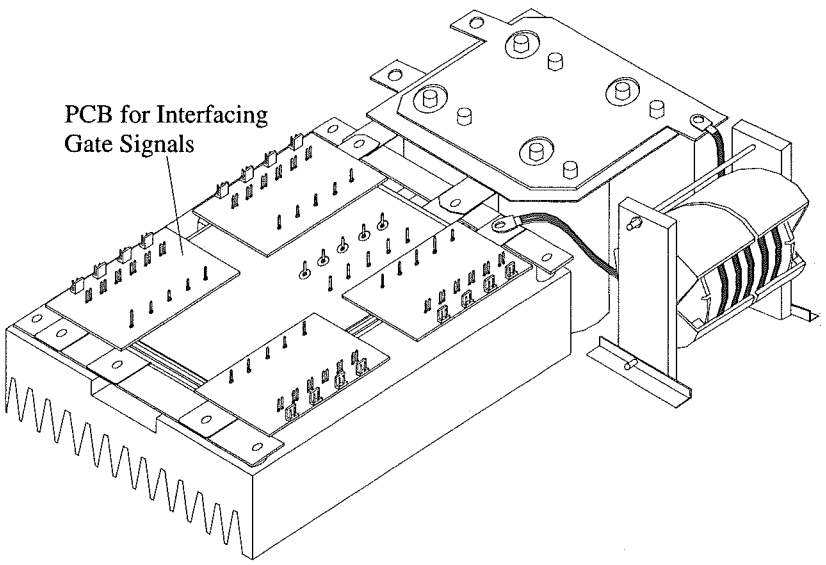


Figure 5.7. Placement of PCBs for interfacing the gate signals.

In Figure 5.8 it is seen that four gate drive PCBs were installed on a large insulating board, which completely cover the laminated bus and prevent any metal objects from coming into contact with the bus bars. This insulating board has two slots, through these two slots, the gate signals from the gate drive PCBs can be connected to the interface PCBs with short lengths of twisted pair.

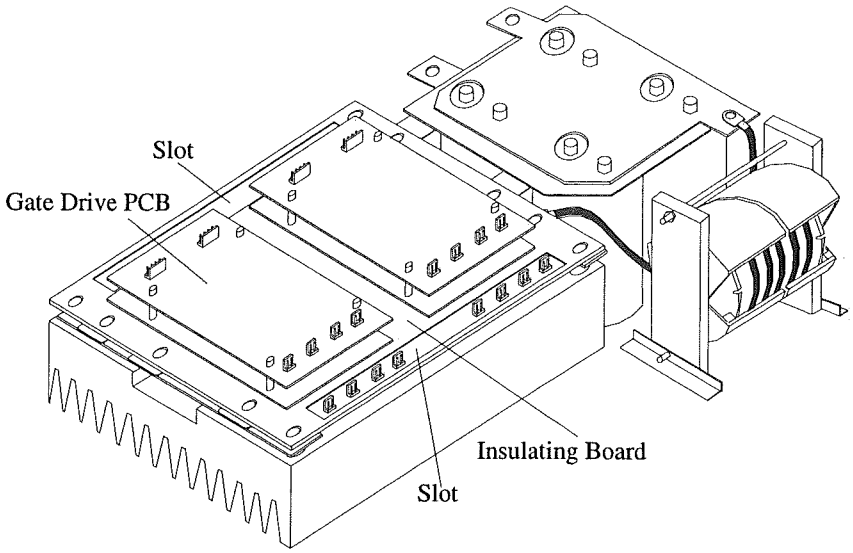


Figure 5.8. Placement of the gate drive PCBs.

The constructed resonant inverter needs to be easily configured as a hard switching inverter so that an experimental evaluation of the losses in the resonant and hard switching inverter can be conducted with the same inverter devices. Figure 5.9 shows the configuration as the hard switching inverter. The resonant inductor was removed and replaced with a copper conductor, the clamp capacitors were disconnected from the clamp device, and the gate drive PCB for the clamp device was removed.

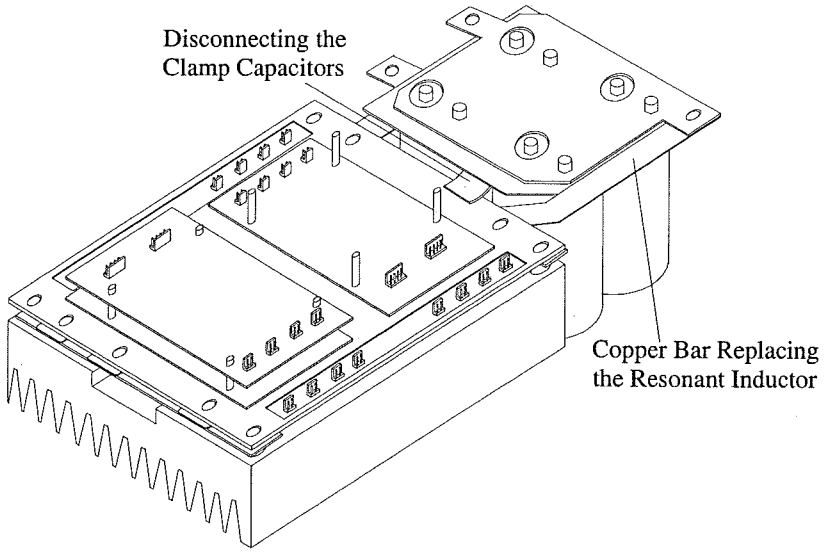


Figure 5.9. Configuration as a hard switching inverter.

5.3 Summary

In this chapter, the resonant inductor has been designed based on an available core and Litz wires. The designed resonant inductor has low winding losses and relatively large core losses due to the overly large core and the limited number of turns, but it is still acceptable for the resonant inverter application. Five polypropylene capacitors connected in parallel were used to form the resonant capacitor. Two electrolytic capacitors were used to form the clamp capacitor. For the switches, 50A/600V IGBT modules were chosen as the inverter devices and the clamp device, with the top and bottom three IGBTs in each module paralleled to obtain the required current rating. By minimizing the interconnection distance between the components and incorporating a laminated bus structure into the assembly, the stray inductance in the constructed resonant inverter was minimized. The prototype resonant inverter can be easily configured as a hard switching inverter. In the next chapter the resonant link control circuit for maintaining the link resonance and limiting the bus voltage is detailed.

CHAPTER 6

RESONANT LINK CONTROL

This chapter describes the circuits used to control the resonant operation of the resonant DC link inverter. The overall control circuit consists of the sub-circuits for the resonant inductor charging control, active clamping control, and inverter protection. The auxiliary circuits used to precharge the clamp capacitor and initiate the link resonance are also described briefly.

6.1 Inductor Charging

6.1.1 Operating Principle

When the resonant DC link inverter operates with a three-phase load, the resonant link can be subjected to severe inverter DC current transitions. In order to maintain link resonance, it is necessary to ensure that a proper initial current is established in the resonant inductor at the beginning of every resonant cycle. The inductor charging control circuit is developed for this purpose. The required initial current is given by Equation 6.1.

$$I_{Lr}(0) = I_X + I_T(\min) \tag{6.1}$$

I_X is the inverter DC current in the next resonant cycle, and can be assumed to be constant for one resonant cycle. $I_T(\min)$ is the minimum trip current required to overcome the link losses and guarantee the return to zero of the bus voltage at the end of the next resonant cycle. In the resonant inverter the transitions of the inverter DC current occur only at the zero crossings of the bus voltage because the inverter devices are only switched at zero crossings in order to obtain zero voltage switching. This feature makes it possible for the control circuit to predict the inverter DC current for the next resonant cycle before the zero crossing. A predicted inverter DC current,

denoted as I_x^*, then replaces I_x in Equation 6.1 and provides a reference signal for the inductor charging control [Deshpande, 1997].

A block diagram of the inductor charging control is shown in Figure 6.1, and the associated waveforms are shown in Figure 6.2. The resonant bus voltage, v_{cr}, is compared to a reference voltage, V_{check}. Whenever the bus voltage is less than this reference voltage, a sampling pulse, P_{sample}, is generated. Sinusoidal PWM signals, A+, A-, B+, B-, C+ and C-, are sampled and held prior to the zero crossing by means of a flip-flop (FF1) clocked with the sampling signal P_{sample}. In this way, the new switching pattern of the inverter for the next resonant cycle is known beforehand.

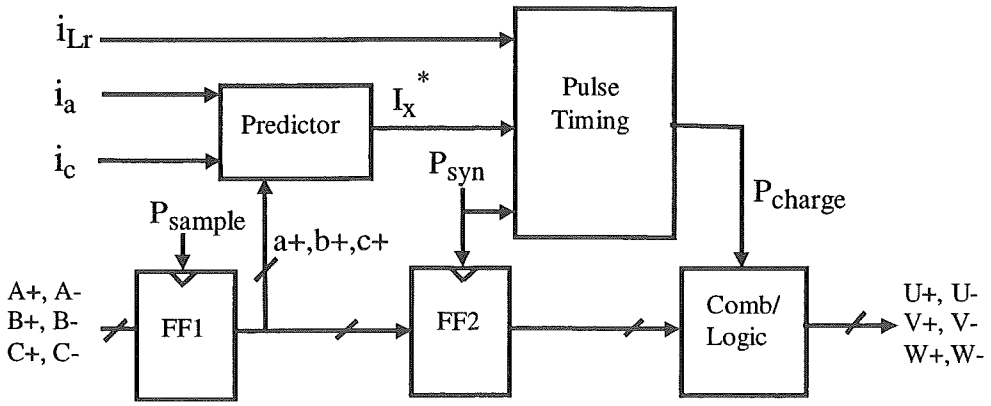


Figure 6.1. Block diagram of inductor charging control.

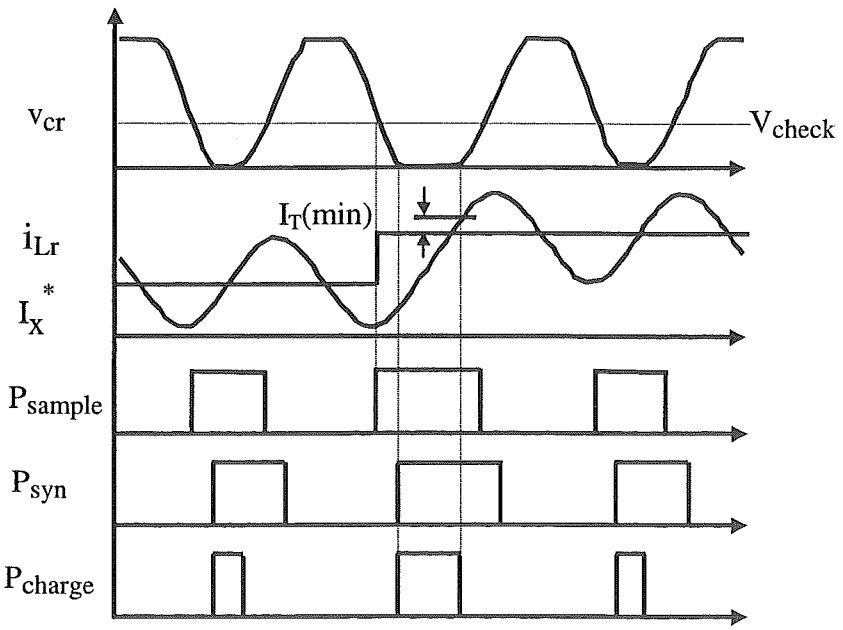


Figure 6.2. Waveforms for the current prediction scheme.

The sampled PWM signals, a+, b+ and c+, are then fed to an inverter DC current predictor. This predictor is also supplied with motor currents, i_a and i_c. By knowing the new switching pattern of the inverter and the information regarding the motor currents, the predictor yields the predicted inverter DC current, I_X^*, before the zero crossing as shown in Figure 6.2.

When the bus voltage reaches zero volts, a pulse, P_{syn}, is produced. This pulse is used to transfer the sampled PWM signals (a+, b+ and c+) to a combination logic circuit by means of a second flip-flop (FF2). At the same time, this pulse triggers a timing circuit that generates an inductor charging pulse, P_{charge}. Through a combination logic circuit and IGBT gate drives, this inductor charging pulse is applied to all the inverter devices to accomplish the bus shorting. The inductor current, i_{Lr}, is linearly ramped with the shorted bus, and the control circuit continuously compares the inductor current with the predicted inverter DC current. Once the inductor current is larger than the predicted inverter DC current by a value of the minimum trip current, $I_T(min)$, the control circuit terminates the inductor charging pulse immediately and releases the bus shorting. Upon releasing the bus shorting, the gate drive signals are updated with the new switching pattern, and the resonant inverter begins the next resonant cycle.

6.1.2 Current Prediction

The circuit diagram of the inverter DC current predictor is shown in Figure 6.3. It consists of two ICs. IC8 (4051) is an eight-channel analog multiplexer having three binary control inputs. The three binary control inputs select one of the eight channels to be turned on, and connect one of the eight analog inputs to the output (pin 3). The three binary control inputs are supplied with the sampled PWM signals, a+, b+ and c+. All of the eight analog inputs are supplied with the appropriate current signals according to Table 6.1, which is determined by the switching functions (Equation 2.2 in Section 2.1.2).

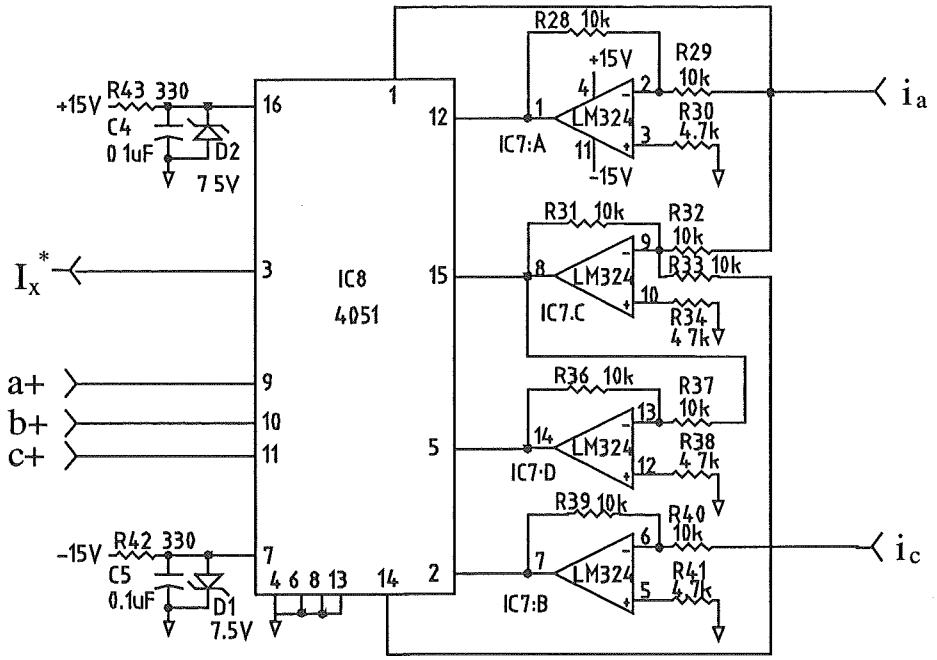


Figure 6.3. Circuit diagram of the inverter DC current predictor.

Table 6.1 Multiplexer Current Signals

Binary Inputs			Selected Channel	Output I_x^*
a+	b+	c+		
0	0	0	13	0
0	0	1	14	i_c
0	1	0	15	i_b
0	1	1	12	$-i_a$
1	0	0	1	i_a
1	0	1	5	$-i_b$
1	1	0	2	$-i_c$
1	1	1	4	0

Load currents, i_a and i_c, are measured using hall-effect current sensors (LA100-S/SP1, LEM) that are placed in the inverter output. Whereas the current i_b is constructed from the measured currents i_a and i_c under the assumption that the sum of the three currents is zero in a balanced three-phase system. The required summation and inversion of the current signals are obtained with the help of four operational

amplifiers IC7 (LM324). The outputs of these amplifiers are connected to the various channels of the multiplexer. Channels 4 and 13 are supplied with a zero voltage since these channels correspond to the freewheeling state of the inverter. The sampled PWM signals select the proper channel, and the corresponding current signal appears at output of IC8, giving the predicted inverter DC current, I_X^*. The waveform of signal I_X^* is a replica of the actual inverter DC current. However, since the PWM signals are sampled before the zero crossing, the predicted signal I_X^* provides advance information regarding the actual inverter DC current. Experimental waveforms showing the operation of the inverter DC current predictor are given in Figure 8.10 in Section 8.2.4.

6.1.3 Charging Control

The circuit used for controlling the inductor charging pulse is shown in Figure 6.4. The resonant bus voltage, v_{cr}, is measured using a resistor divider (R3 and R4). A high input impedance operational amplifier (IC2, TL071) is connected as a voltage follower so that the output of the amplifier is proportional to the resonant bus voltage. In the same manner the supply voltage, V_S, is measured. An operational amplifier (IC5, LM318), connected as a comparator, compares the measured bus voltage with a reference voltage, V_{check} (refer to Figure 6.2). This reference voltage varies with the supply voltage so that the control circuit functions correctly even when the supply voltage is changed. When the bus voltage is lower than the reference voltage, the output of the comparator goes high, producing the pulse signal, P_{sample}, to sample the PWM signals. To ensure that the predicted current is obtained before the zero crossing, it is essential that the operational amplifier (IC5) have a high slew rate.

By delaying the signal P_{sample} via IC10 (4073) and a RC network (R26 and C1) the second pulse, P_{syn}, is obtained. With appropriate adjustment of R26 and C1 the signal P_{syn} can be tuned to go high once the bus voltage reaches zero volts. The pulse P_{syn} is used to synchronize the sampled PWM signals with the zero crossing of the

bus voltage. Meanwhile, it triggers a timing circuit (IC11, 4098, Monostable) that generates the inductor charging pulse, P_{charge}, at pin 10 of the IC11. A RC network (VR1, R47 and C2) controls the maximum pulse width of the inductor charging pulse. However, the charging pulse is terminated immediately with a low-level signal at pin 13 of IC11. The inductor current, i_{Lr}, is measured using a hall-effect current sensor (LA100-S/SP1, LEM). An operational amplifier (IC6, LM318), connected as a comparator, compares the difference between the inductor current and the predicted inverter DC current, I_X^*, with the minimum trip current, which is determined by the supply voltage and resistors (R21 and R22). When the inductor charging pulse is produced and applied to all the inverter devices, the bus is shorted and the inductor current is increased towards the required current. Once the inductor current is larger than the predicted inverter DC current plus the minimum trip current, the output of the comparator (IC6) goes low and terminates the inductor charging pulse.

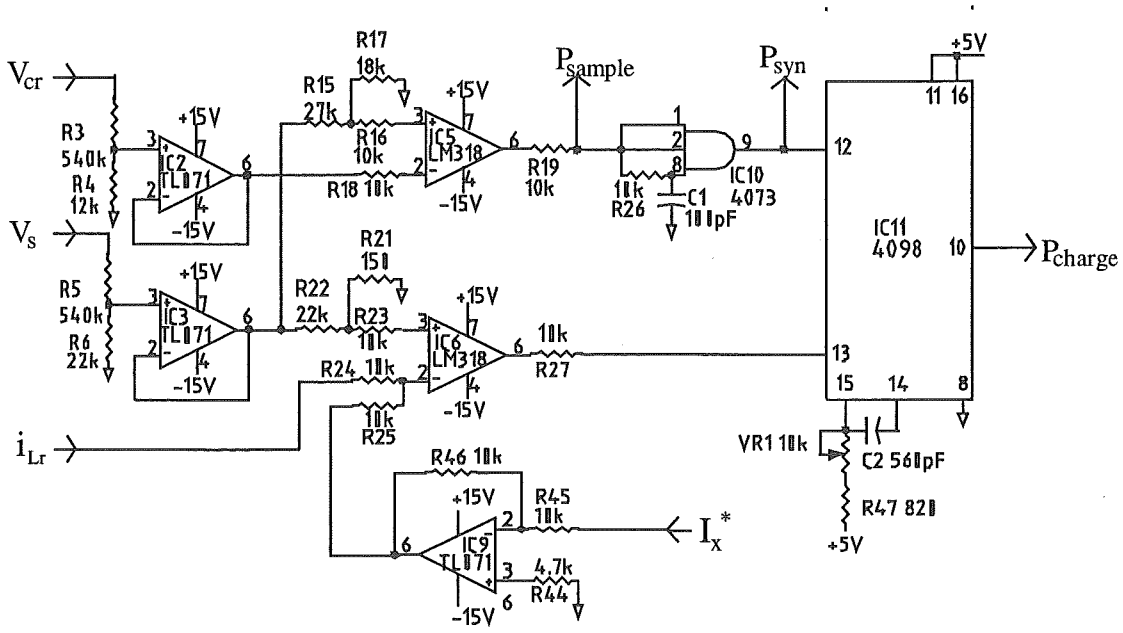


Figure 6.4. Circuit used for controlling the inductor charging pulse.

When the resonant inverter is under no load, the pulse width of the inductor charging pulse is same for each resonant cycle, and it can be adjusted as required by varying the setting of the minimum trip current (R21 and R22) and the maximum pulse width (VR1, R47 and C2).

6.1.4 Sampling and Synchronizing PWM Signals

The circuit for sampling and synchronizing PWM signals is shown in Figure 6.5. For the sake of clarity, only one phase circuit is given. The sinusoidal PWM signals A+ and A- generated by comparing a triangular waveform with a sinusoidal reference waveform, are sampled by means of a dual flip-flop (IC12, 4013). These sampled PWM signals, representing the new switching pattern, are held at the output pins 1 and 13 of IC12 to predict the inverter DC current. When the bus voltage reaches zero, the new switching pattern is transferred to the output of a second flip-flop (IC13, 4013). During the bus-shorting interval, the inductor charging pulse drives all the inverter devices. Upon releasing the bus shorting, the new switching pattern takes over the control of the inverter devices, and according to the new switching pattern all outgoing devices are turned off and the inverter is then switched to the new state.

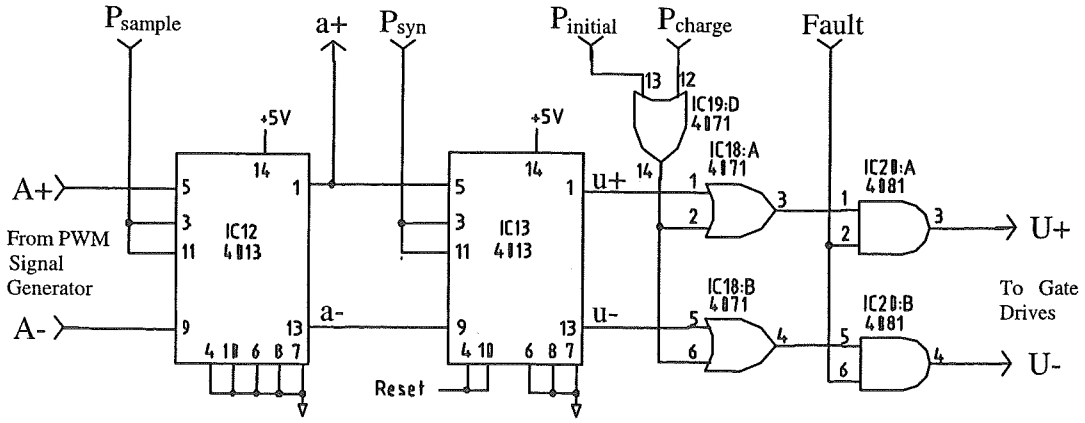


Figure 6.5 Circuit for sampling and synchronizing PWM signals.

6.2 Active Clamping

The purpose of the active clamping is to limit the peak bus voltage to an acceptable level. This is accomplished by ensuring charge balance on the clamp capacitor through the control of the clamp device. Figure 6.6 shows the circuit for the active clamping control. The resonant bus voltage and the supply voltage are measured using the resistor dividers in conjunction with the voltage followers. An operational amplifier (IC4, LM318), connected a comparator, compares the bus voltage with a reference voltage, which is determined by the supply voltage and resistors (R11 and R13). When the bus voltage is larger than the reference voltage, the output of the comparator goes high and triggers a timing circuit (IC11, 4098, Monostable). The timing circuit generates a clamp pulse, P_{clamp}, to turn on the clamp device. By adjustment of the reference voltage it can be made that this clamp pulse is applied to the clamp device only when the clamp diode is conducting. A RC network (VR2 and C3) controls the pulse width of P_{clamp}. By varying the pulse width the clamping voltage level can be varied accordingly, thus the required clamping voltage can then be obtained.

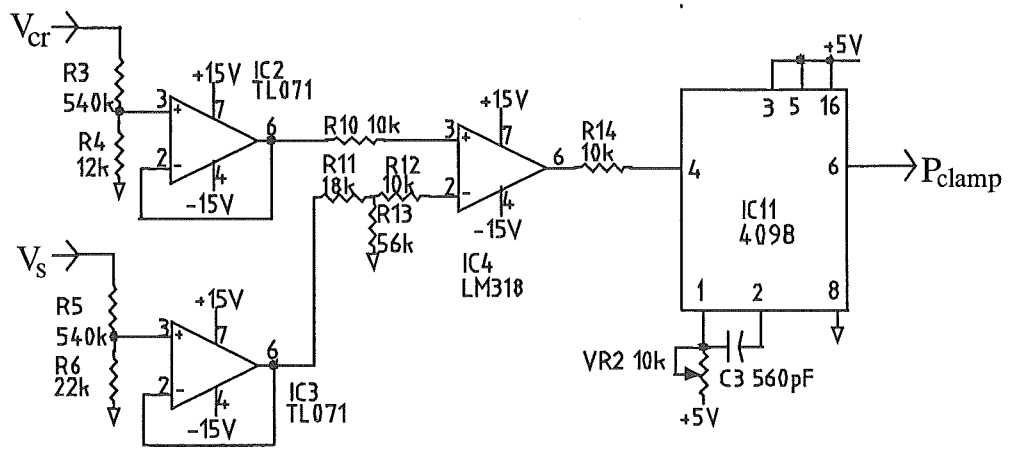


Figure 6.6. Circuit for the active clamping control.

6.3 Protection

The resonant inverter must be protected from any fault conditions that may occur. These fault conditions include:

- overvoltage on the DC supply, clamping voltage, and resonant bus voltage,
- overcurrent in the motor and resonant inductor,
- de-saturation of the inverter and clamp IGBTs,
- resonance failure.

Whenever one of these fault conditions is detected, the protection circuit produces a latched "Fault" signal (low-level active) to turn off all the switching devices and prevent the resonant inverter from being damaged. In this section, the protection circuit for the resonance failure is detailed.

Resonance failure means that the resonant bus voltage does not return to zero after one resonant cycle. This situation may occur when the required initial current in the resonant inductor is not established. Should resonance failure occur, the gate signals of the inverter devices will remain unchanged, since the control circuit will fail to produce the pulse (P_{syn}) to forward the new switching pattern to the gate drives (refer to Figure 6.5). Under this circumstance, the motor will be subjected to a DC voltage continuously, and the motor currents will rise to a high level and may destroy the inverter IGBTs, as the motor currents will be only limited by the winding DC resistance.

This resonance failure situation must be detected so that the resonant inverter can be shut down to avoid being damaged. Figure 6.7 shows the circuit for detecting resonance failure. In this circuit, IC13 is the second flip-flop used to synchronise the sampled PWM signals with the zero crossing (see Figure 6.5). Two PWM signals for one phase gate drives, u+ and u-, are monitored separately with two charging-discharging RC circuits. Under normal operation these signals toggle between two polarities (low and high levels), as they are updated with the new switching signals as long as the link is resonating. The voltages across two capacitors (C6 and C7) are lower than a reference voltage set by R50 and R51. The outputs of two operational amplifiers (IC27:A and IC27:B, TL072) remain low, and the output of IC32 (4043,

R/S Latches) stays high. When the resonance failure occurs, one of the PWM signals (u+ and u-) will remain a high level and unchanged. One of the two capacitors will be fully charged so that one of the two operational amplifiers will toggle to a high level output. A latched signal (low level) indicting resonance failure will appear at the output of the latch.

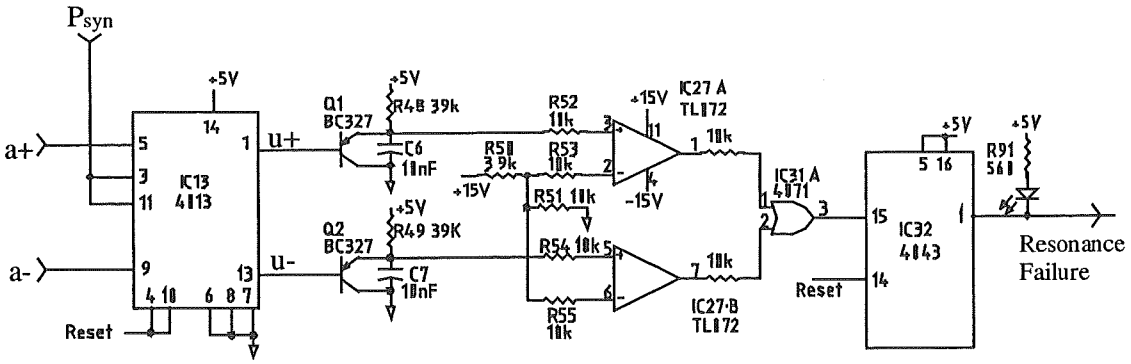
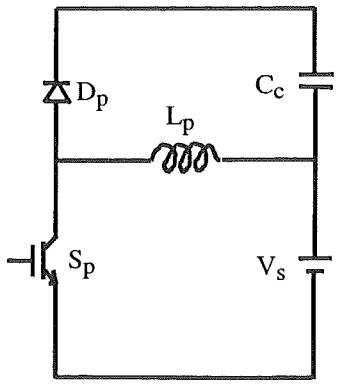


Figure 6.7. Circuit for detecting resonance failure.

6.4 Auxiliary Circuits

6.4.1 Precharge

The clamp capacitor has to be charged before resonance of the link is possible. The circuit for precharging the clamp capacitor is shown in Figure 6.8. In this circuit, when the IGBT (S_p) is conducting, energy is built up in an inductor (L_p). When the IGBT is turned off, the induced voltage across the inductor forces a diode (D_p) into conduction, and the stored energy in the inductor is then delivered to the clamp capacitor (C_c). By repeated switching of S_p, the required clamping voltage, KV_s, can be obtained. The IGBT is driven by a switching signal with a frequency of 20kHz and a duty ratio of 0.2. The precharge circuit is only activated at inverter start-up; thus components with low power ratings are sufficient. The precharge circuit is shut down just before the link resonance is initiated.



L_p: 2.5mH, 3C85 R14, 80T, 0.8mm air gap

S_p: IGBT, BUK854-800A, 800V/12A

D_p: MUR860, 600V/6A

Figure 6.8. Circuit for precharing the clamp capacitor.

6.4.2 Resonance Initiation

After the resonant inverter power-on, the resonant capacitor voltage is equal to the DC supply voltage and no energy is stored in the resonant inductor, so that the bus voltage can neither resonate to the clamping voltage nor to zero. The link resonance has to be initiated manually by producing an initial downward swing of the bus voltage. This is accomplished by generating an initial inductor charging pulse, $P_{initial}$, to turn on all the inverter devices for a very short period. Figure 6.9 shows the circuit for initiating the link resonance. Once a "START" button is pressed, a pulse is generated at pin 6 of IC34:A (4098, Dual Monostable). The latch (IC35, 4043) catches the leading edge of this pulse, and the output of this latch is used to shut down the precharge circuit. At the trailing edge of this pulse, the initial inductor charging pulse, $P_{initial}$, is produced at pin 10 of IC34:B and sent to the gate drives to short the bus initially. Resistors R87 and C8 control the pulse width of $P_{initial}$.

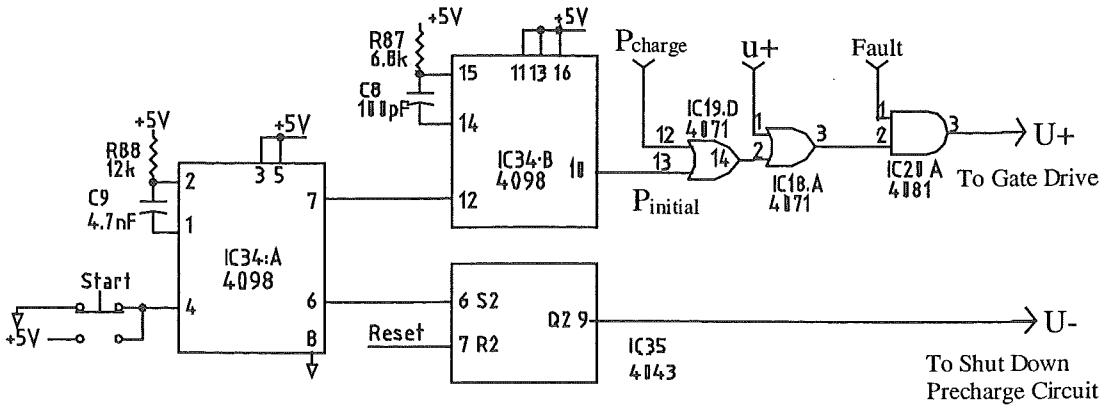


Figure 6.9. Circuit for initiating the resonance of the link.

6.5 Summary

This chapter has described the details of the control circuit used to control the resonant DC link inverter. The inductor charging control is for maintaining the link resonance. The inverter DC current in the next resonant cycle is predicted and used as a reference for the inductor charging control so as to establish the required initial current in the resonant inductor. The active clamping control is for limiting the bus voltage. The preset clamping voltage is maintained by controlling the conduction time of the clamp device. Resonance failure of the resonant link results in the unchanged PWM switching signals for the inverter devices, and it is detected by monitoring the pulse width of the switching signal to protect the resonant inverter from being damaged.

CHAPTER 7

RESONANT LINK TESTS

In the previous chapters 5 and 6, the design and construction of the prototype resonant DC link inverter has been described, and the resonant link control circuit has been detailed. This chapter presents test results of the resonant DC link inverter under no-load conditions, and the following chapters 8 and 9 present load tests and a performance evaluation of the prototype resonant DC link inverter.

Th resonant DC link is tested extensively at full supply voltage under no-load conditions. The typical operation results of resonant DC link with a minimum trip current and an excessive trip current are given. The power losses in the resonant link are investigated with the link parameters such as the resonant impedance and inductor charging time. The impact of the stray inductance on the operational behavior of the resonant link is discussed, and an experimental comparison showing a substantial reduction of the stray inductance in the prototype resonant inverter is included.

7.1 Experimental Setup

Experimental setup for resonant link tests is shown in Figure 7.1. DC power is supplied to the resonant DC link through a rectifier from a variac, which allows the supply voltage to be varied. The resonant link control circuit described in Chapter 6 is used to control the resonant operation. Under no-load conditions, all devices in the inverter stage can be treated as a single device, denoted as S_m for IGBTs and D_m for anti-parallel diodes. At the beginning of each resonant cycle, the control circuit generates an inductor charging pulse (refer to Figure 6.4), and S_m is turned on

for an inductor charging time, t_s, allowing the current in the resonant inductor to be ramped up to a trip current, I_T. After turn-off of S_m, the bus voltage resonates towards the clamping voltage, KV_s. With the clamp diode D_c conducting, the control circuit produces a clamp pulse (refer to Figure 6.6), and the clamp device, S_c, is turned on for a conduction time, t_c, allowing energy transferred to the clamp capacitor to be fed back to the resonant tank. By adjusting the inductor charging time, the trip current can be varied as required for the tests. The required clamping voltage is set by a proper conduction time of S_c.

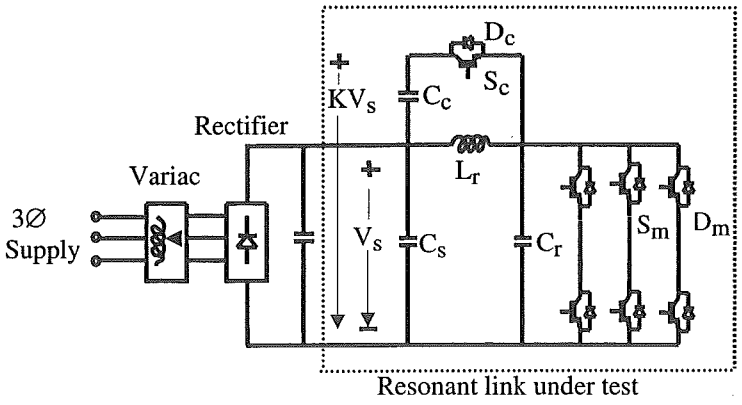


Figure 7.1. Experimental setup for the resonant link tests.

7.2 Resonant Link Operation

7.2.1 Resonance Initiation

To initiate the link resonance after power-on, the "START" button in the control circuit is pressed, and an initial inductor charging pulse is generated (refer to Figure 6.9). This charging pulse is then used to produce an initial downward swing of the bus voltage by shorting the bus via the inverter devices. The measured waveforms in Figure 7.2 shows the startup of link resonance at the nominal supply voltage of 240V DC. Once the initial bus shorting is released, the energy stored in the resonant inductor during the initial charging makes the bus voltage return to zero volts after one resonant cycle. Then the regular resonant operation begins, and link resonance is maintained automatically by the control circuit. The initial charging pulse used for

this test is about 1.5μs. Note that the initial bus shorting is actually a hard switching event. Since considerable energy is stored in the resonant capacitor before link resonance is initiated, shorting it to the ground may cause a large current to flow through the inverter devices. According to the simulation, based on the actual implementation of the resonant link, the peak current flowing through the inverter stage during the initial bus shorting is about 160A. With three phase legs paralleled to accomplish the bus shorting, the inverter stage has a rated current rating of 450A, which is large enough to cope with this peak current without causing de-saturation of the inverter devices.

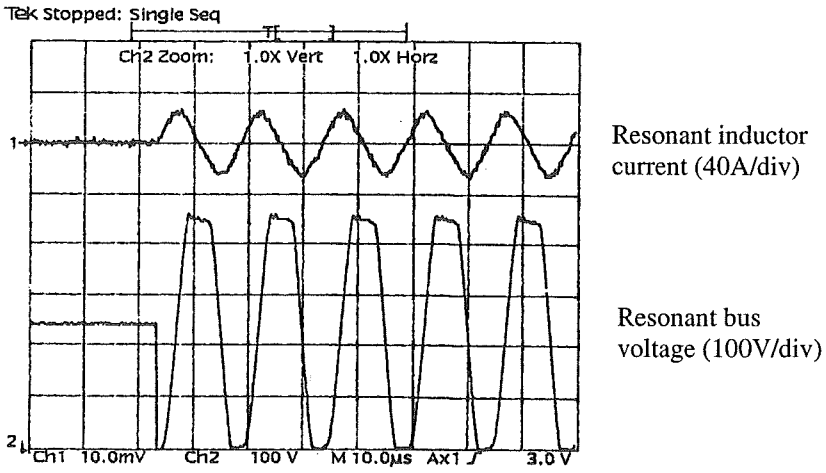


Figure 7.2. Resonance initiation.

7.2.2 Link Waveforms

Figure 7.3 displays the measured waveforms of the resonant inductor current and bus voltage for the resonant DC link with the active clamping disconnected. For this test, the supply voltage is set to 240V, the resonant inductor is 20.45μH, and the resonant capacitor is 0.234μF. This makes the resonant impedance 9.35Ω and there is a natural resonant frequency of 72.7kHz.

Waveforms in Figure 7.3 are produced when the inductor charging time t_S is reduced to a minimum value (about 0.5μs). If the time is reduced lower than this value then the resonant operation could not be sustained, and this corresponds to a minimum trip current I_T(min) of about 6A in the resonant inductor. Under this minimum excitation,

the resonant inductor current and bus voltage are nearly pure sinusoids, and the measured resonant frequency is 72kHz close to the natural resonant frequency of 72.7kHz. The measured rms current in the resonant inductor is 18.5A and fairly close to the calculated value of 18.2A given by $0.707V_S/Z_r$. The peak bus voltage is 488V, only a few volts above $2V_S$, and it maintains a constant value from cycle to cycle for the resonant link under no-load.

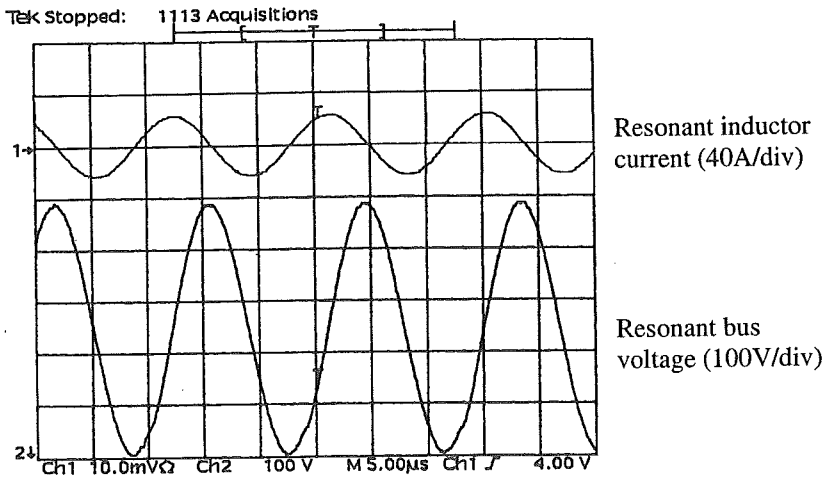


Figure 7.3. Resonant link waveforms with the active clamping disconnected.

Figure 7.4 below shows the measured waveforms of the resonant inductor current and bus voltage for the actively clamped resonant DC link. For the measurements, the supply voltage is 240V, and the clamping voltage is 440V. The trip current in the resonant inductor is increased above the minimum trip current found from the test in

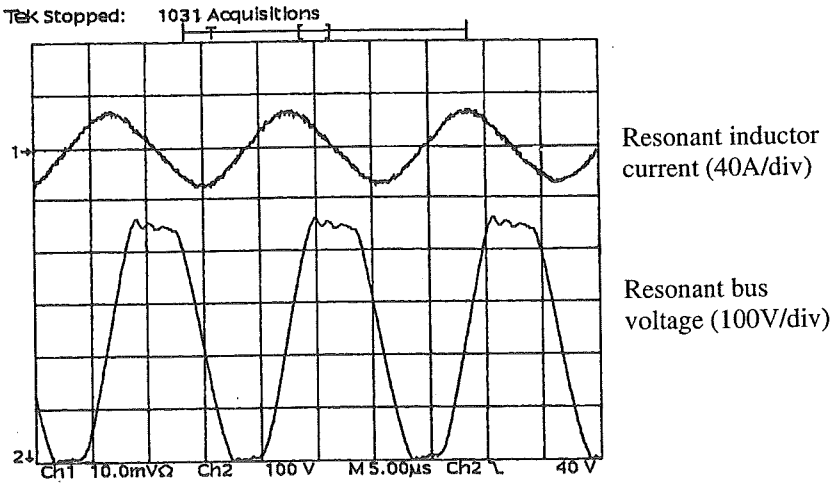


Figure 7.4. Resonant link waveforms for the actively clamped resonant DC link.

Figure 7.3. Due to a larger initial current in the resonant inductor, there is excessive energy circulating in the resonant link causing the resonant inductor current to increase to 20.5A rms, and the resonant frequency drops to about 64kHz. Under this over-excited circumstance, the active clamping is necessary to limit the bus voltage. The measured peak bus voltage is 455V, which is well below the 600V IGBT blocking voltage constraint. The typical value of the dv/dt of the resonant pulses is 100V/μs. The small oscillations in the bus voltage waveform during the active clamping observed in Figure 7.4 are caused by the stray inductance, and this is discussed later in this chapter.

7.2.3 Zero Voltage Switching

The purpose of adding the resonant link to a conventional hard switching inverter is to create zero voltage switching conditions for the devices connected across the resonant bus, including the clamp device in the actively clamped resonant DC link. Figures 7.5 and 7.6 demonstrate such switching conditions for the main device and clamp device respectively. For all the measurements, the supply voltage is 30V, the resonant inductor is 20.45μH, and the resonant capacitor is 0.234μF. Since some measurements are not accessible in the final implementation of the resonant inverter due to the low stray inductance construction, the waveforms presented in Figures 7.5 and 7.6 are measured from an earlier experimental resonant link. In this earlier link a single IGBT module replaces the inverter stage shown in Figure 7.1, and the stray inductance in the resonant circuit is not particularly minimized.

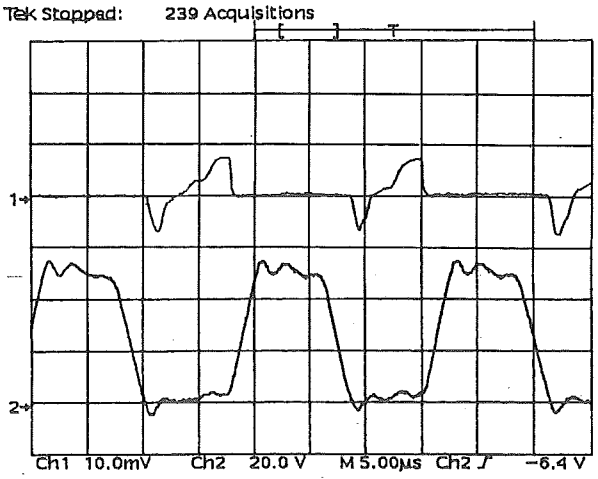


Figure 7.5. Zero voltage switching conditions for the main device.

The top trace in Figure 7.5 is the current flowing through the main device (S_m and D_m), and the bottom trace is the resonant bus voltage. As shown, the anti-parallel diode, D_m, conducts first when the bus voltage reaches zero volts, shorting the bus for a while. Then, the main device, S_m, is turned on under a zero voltage switching condition to charge the resonant inductor. Upon turning off of S_m the bus voltage increases at a low dv/dt as a result of the resonant action. From Figure 7.5 it is clearly seen that virtually there is not the simultaneous presence of the current and voltage on the device, indicating very low switching loss.

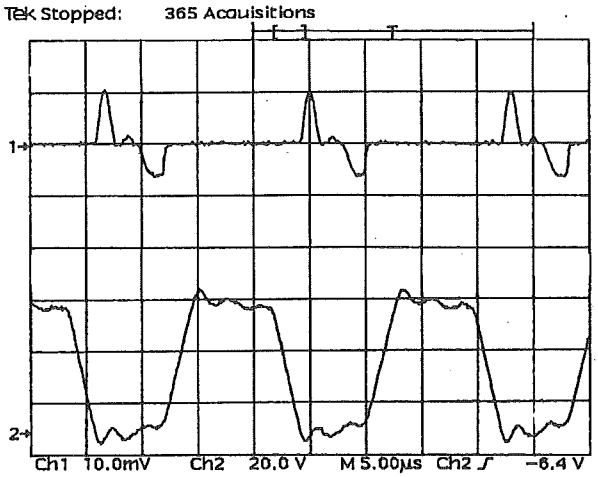


Figure 7.6. Zero voltage switching conditions for the clamping device.

Shown in Figure 7.6, the top trace is the current flowing through the clamp device (S_c and D_c), and the bottom trace is the voltage across the clamp device. Once the bus voltage reaches the clamping voltage, diode D_c conducts first and clamps the bus voltage to the clamping voltage. Then S_c is turned on under a zero voltage switching condition. After turn-off of S_c the bus voltage resonates down to zero, and the voltage across the clamp device increases at a low dv/dt. Similarly, there is not the simultaneous presence of the current and voltage on the clamp device.

From the measurements above, it has been shown that in the resonant DC link inverter all devices are turned on only when the anti-parallel diodes are conducting, therefore the turn-on losses are negligible. The turn-off losses are greatly reduced because of the soft increase of the device voltage [Mertens, 1990].

7.2.4 Resonant Link ESR

Figure 7.7 gives the DC link waveforms just after all devices are turned off in the final implementation of inverter hardware with a supply voltage of 30V.

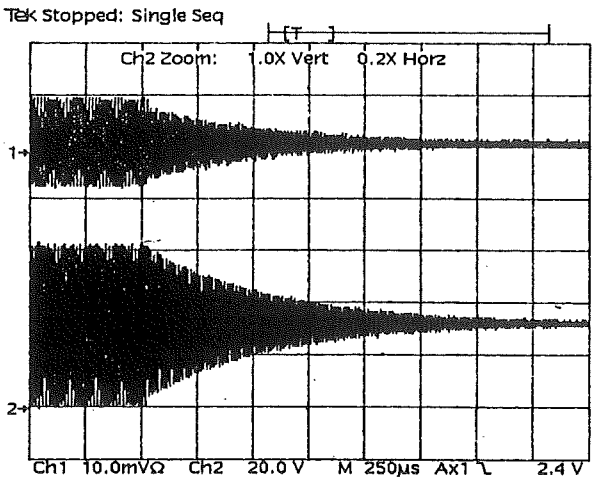


Figure 7.7. Resonance termination (L_T=20.45µH, C_T=0.234µF, and Z_T=9.35Ω).

This test provides an easy method to estimate the total series equivalent resistance R_S in the resonant link. Here, R_S includes all ESRs from the resonant inductor, resonant capacitor, supply capacitor (C_S), and interconnection conductors. Looking at the bus voltage, the bottom trace, in Figure 7.7, it takes 1750µs to decay to the supply voltage. The time constant can be estimated as 350µs, and R_S of the resonant link is then able to be calculated to be approximately 58.4mΩ, thus giving a quality factor of the resonant link of 160.

7.3 Resonant Link Losses

Total inverter losses under no-load conditions give a good indication of losses in the resonant tank and clamp device under most operating conditions. The DC input power is used as a measure of these losses.

7.3.1 Inductor Charging Time

Resonant link losses were measured against the supply voltage for the different inductor charging time of 1.1, 1.5, and 2.0μs, respectively. The results are plotted in Figure 7.8. For all measurements, the resonant inductor is 20.45μH, and the resonant capacitor is 0.234μF, giving a value of the resonant impedance of 9.35Ω.

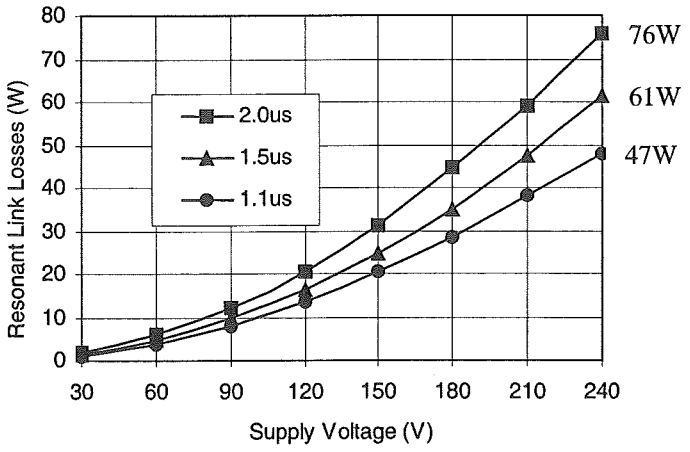


Figure 7.8. Link losses for the different inductor charging time t_s.

Power losses in the resonant link are seen to be fairly sensitive to the inductor charging time. For instance, increasing the inductor charging time from 1.1μs to 2μs causes the link losses to go up by 62%. Therefore with a loaded resonant inverter the inductor charging time should be controlled as short as possible provided that the link resonance is maintained. Otherwise, the link losses may be more than the switching losses eliminated in the inverter stage.

7.3.2 Resonant Impedance

Resonant link losses were evaluated for the following combinations of the resonant inductance and capacitance: (L_r=10.14μH, C_r=0.494μF), (L_r=15.16μH, C_r=0.323μF), and (L_r=20.45μH, C_r=0.234μF), these combinations correspond to the resonant impedance values of 4.5, 6.81 and 9.35Ω, respectively. Each combination gives a same natural resonant frequency of about 72kHz. These inductance values were obtained by adjusting the air gap and the number of turns of the inductor winding, and the capacitance values were obtained by paralleling different numbers of polypropylene capacitors, each with a value of 0.047μF. Link losses were measured against the supply voltage with these different values of the resonant impedance. The experimental results are plotted in Figure 7.9. For all the measurements, the inductor charging time was set to 1.1μs.

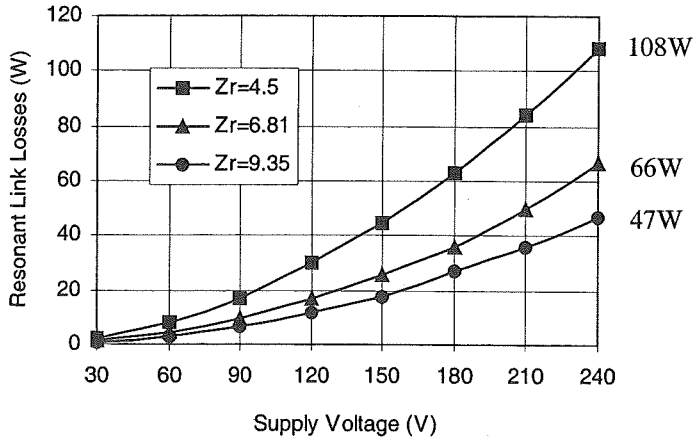


Figure 7.9. Link losses for different values of the resonant impedance.

It can be seen that resonant link losses are very strongly dependent on the resonant impedance. Typically, power losses of 47W are incurred in the resonant link in order to sustain the resonant operation with the resonant impedance of 9.35Ω at full supply voltage of 240V DC.

7.4 Stray Inductance

Minimizing the stray inductance in a resonant DC link inverter is a critical area since the stray inductance effects are amplified by the high frequency operation. The simulations of the actively clamped resonant DC link modeled with the stray inductances have been performed in Section 3.3. Major elements of the stray inductance, which contribute parasitic oscillations in the bus voltage during the active clamping and the bus shorting intervals, have been identified through the simulations. In Chapter 5 it has been shown that the laminated bus structure was used for the construction of the prototype resonant DC link inverter and the interconnection distances of the link components were minimized to reduce the stray inductance.

Figure 7.10 shows the link waveforms measured from an earlier implementation of the resonant link, where the stray inductances were not particularly minimized. For the measurement in Figure 7.10, the resonant components and the clamping voltage are the same as in Figure 7.4. It can be seen from Figure 7.10 that parasitic oscillations appear in the bus voltage waveform during the active clamping. The peak bus voltage is 480V, an overshoot of 40V above the clamping voltage of 440V. This is a 9% overshoot above the clamping voltage. Parasitic oscillations also exist in the bus voltage waveform during the bus shorting. Voltage oscillations above zero volts during the bus shorting may lead non-zero voltage switching of the inverter devices.

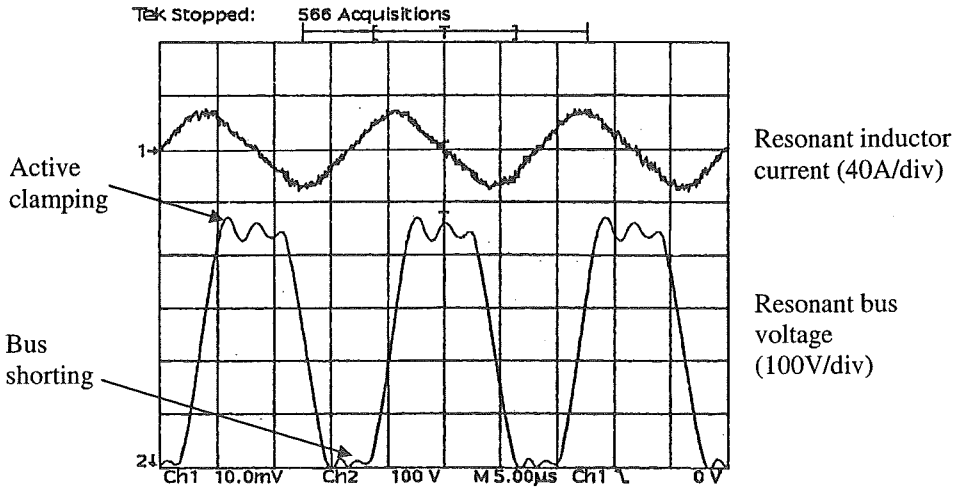


Figure 7.10. Measured waveforms from an earlier implementation of the resonant link.

The parasitic oscillations observed in Figure 7.10 are caused by the interaction between the resonant capacitor and the stray inductances as discussed in Section 3.3. In addition, the simulated waveforms of the bus voltage in Figure 3.7 are fairly similar to the measured ones in Figure 7.10.

Presented in the earlier section of this chapter, Figure 7.4 shows the bus voltage waveform measured from the final implementation of the resonant inverter. Comparing the bus voltage waveforms in Figures 7.4 and 7.10, it is seen that the parasitic oscillations during the bus shorting are virtually eliminated in the final implementation by utilizing the laminated bus for the connections of inverter devices and embedding the resonant capacitor directly into the bus. The validity of the stray inductance reduction with the laminated bus is experimentally verified.

The oscillations during the active clamping interval are also greatly reduced in the final implementation (Figure 7.4), where the overshoot voltage is only 15V above the clamping voltage 440V, and this is a lower voltage overshoot of 3% compared to 9% in Figure 7.10. The oscillation frequency during the active clamping in Figure 7.10 is about 480kHz, and is close to the simulated value of 420kHz in Figure 3.7. It is also noticed that this oscillation frequency is about half of that in Figure 7.4. This indicates that the total stray inductance associated with the active clamping path, $\Sigma L_S(I)$ (refer to Equation 3.1 and Figure 3.6), in the final implementation of the resonant inverter has been substantially reduced to about 25% of that in the earlier implementation. This substantial reduction of the stray inductance is achieved by minimizing the interconnection distances between the components related to the active clamping (refer to Figures 5.2 and 5.3).

7.5 Summary

In this chapter, the prototype resonant DC link inverter has been successfully tested under no-load conditions. Resonant operation has been demonstrated at full supply voltage of 240V DC, the resonant frequency is between 62kHz and 71kHz, and the peak bus voltage is well controlled below 500V with the active clamping. The test results have verified that the constructed resonant inverter has a very low stray inductance. Loss measurements show that power losses of 47W are typically incurred in the resonant link in order to maintain the resonant operation at full supply voltage. In the next chapter, the operational tests of the resonant DC link inverter with a three-phase load are presented.

CHAPTER 8

OPERATIONAL TESTS

This chapter presents the experimental results of the prototype resonant DC link inverter operating with an inductive load and an induction motor. Operation of the resonant link DC under load conditions is discussed. The capability of bidirectional power flow of the resonant DC link inverter is confirmed. An experimental verification of the inverter DC current prediction scheme is included.

8.1 Inductive Load Tests

Experimental setup for the tests of the resonant inverter with a three-phase inductive load is shown in Figure 8.1. A three-phase, moving coil variable inductor was used as the inductive load. The DC supply used for load tests was the same as that used for the resonant link tests in the previous chapter. The synchronized PWM scheme described in Section 6.1.4 was used to modulate the inverter stage. Sinusoidal PWM signals were obtained from a three-phase PWM signal generator developed for this project. This PWM signal generator was designed to have a variable PWM switching frequency of 4kHz to 15kHz, a variable fundamental frequency of 10Hz to 200Hz,

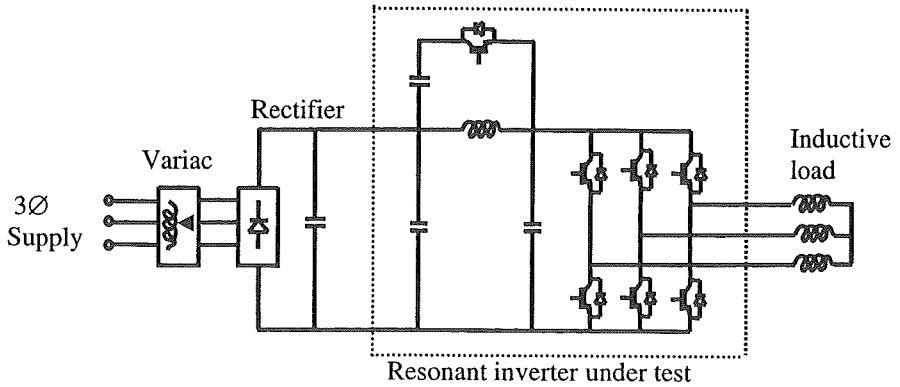


Figure 8.1. Experimental setup for the tests of the resonant inverter with an inductive load.

and an adjustable modulation index. The circuit schematic of this three-phase PWM signal generator is included in Appendix A

Figure 8.2 shows the experimental waveforms of the resonant inductor current and the bus voltage at the nominal supply voltage of 240V, with the resonant inverter delivering an output current of 21.6A rms into the inductive load. Under this operating condition the inductor current is about 19.2A rms, and it is primarily the AC circulating component resulted from the link resonance, as the inverter DC current drawn by the inverter stage with the inductive load is very small. Although the inductor current varies with the changes in the inverter DC current, the resonant pulses of the bus voltage are stable from cycle to cycle, and the peak bus voltage is well restricted below 500V allowing a sufficient voltage margin for the 600V IGBTs connected across the resonant bus. The bus-shorting interval also varies with the inverter DC current, and the average resonant frequency is approximately 70kHz.

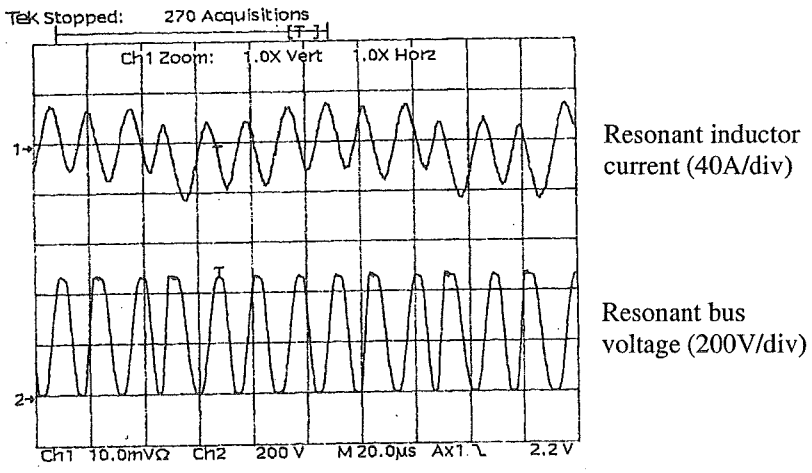


Figure 8.2. Link waveforms of the resonant inverter with the inductive load.

Figure 8.3 shows the output waveforms of the resonant inverter with the inductive load. The upper trace is the output phase current with a fundamental frequency of 50Hz, due to a large value of the load inductance the output current is a clean sinusoid. The lower trace shows the output line-to-line voltage, which is synthesized with the low dv/dt resonant pulses of the bus voltage.

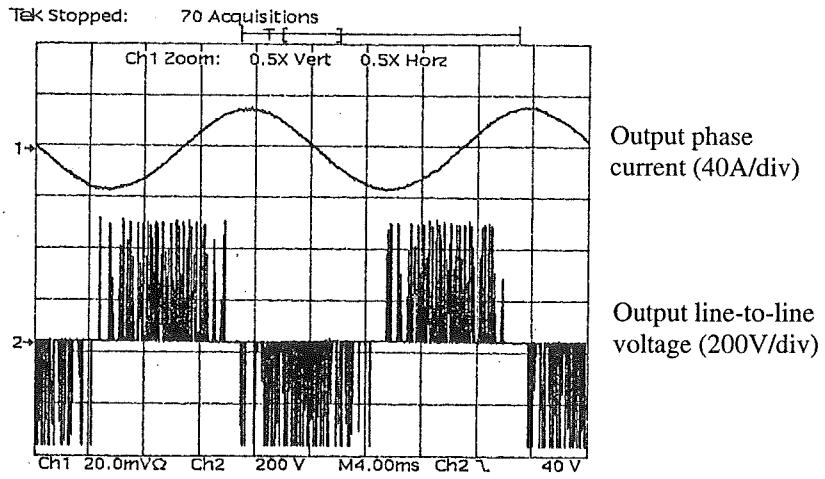


Figure 8.3. Output waveforms of the resonant inverter with the inductive load.

8.2 Motor Load Tests

8.2.1 Experimental Setup

Experimental setup for the tests of the resonant inverter with an induction motor is shown in Figure 8.4. The induction motor can be loaded as required by suspending different weights on the ends of the rope, which is wrapped around a drum coupled to the motor shaft. The induction motor used for the tests has a rated power of 2.2kW, a rated line-to-line voltage of 90V rms, and a rated frequency of 50Hz. [Williams M., 1993].

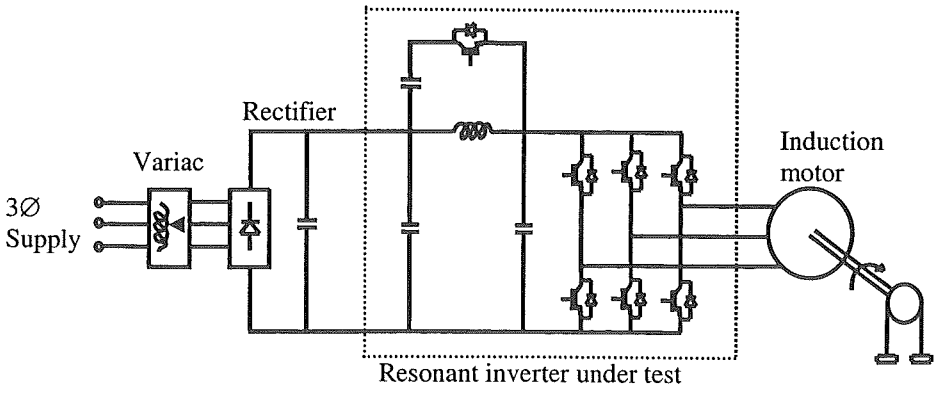


Figure 8.4. Experimental setup for the tests of the resonant inverter with the induction motor.

8.2.2 Motor Start

The motor load tests started with a low supply voltage, and the rope was removed from the drum allowing the motor spinning freely. The fundamental frequency was set to 50Hz, and the PWM switching frequency was set to 4kHz. The motor started rotating once the link resonance was initiated. Typically, DC supply voltage of 37V would make the motor spin freely at full speed. During the startup the induction motor draws a large magnetizing current, thus the inverter DC current is very large compared to the AC resonant current in the resonant link at the low supply voltage. The measured waveforms in Figures 8.5 and 8.6 under this particular operating condition clearly show the operational behavior of the resonant DC link as discussed in Section 2.2.3 (refer to Figures 2.7 and 2.8).

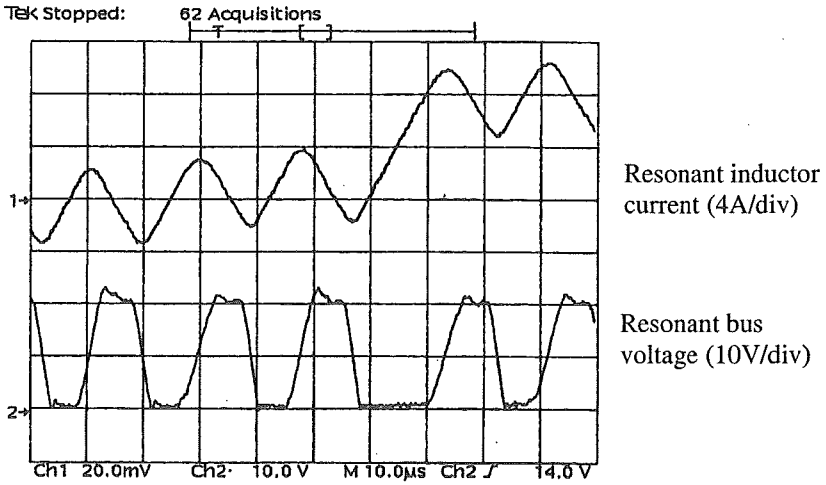


Figure 8.5. Measured link waveforms when the inverter DC current increases.

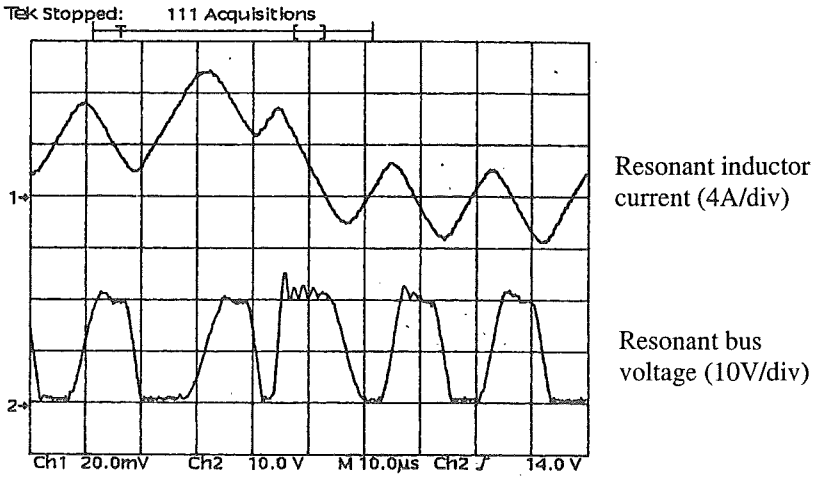


Figure 8.6. Measured link waveforms when the inverter DC current decreases.

It is noticeable from Figure 8.5 that a longer bus-shorting period is required when the inverter DC current increases. The resonant bus remains shorted allowing the inductor current to be built up to the required inverter DC current before the next resonant cycle would start. From Figure 8.6 it can be seen that when the inverter DC current decreases, the bus voltage rises rapidly due to a large initial current flowing into the resonant capacitor. Subsequently, excessive energy is pumped into the clamp capacitor, and causes a larger overshoot of the bus voltage and a longer active clamping period. During the startup of the induction motor the resonant frequency drops to 50kHz, compared to 70kHz measured from the inductive load tests. Figures 8.5 and 8.6 justify an important design rule, that is, the resonant impedance needs to be designed so that the AC resonant current in the resonant link at the nominal supply voltage is at least 25%-30% of the peak load current [Mertens, 1990]. Otherwise the actual resonant frequency would be substantially below the designed value.

Figure 8.7 shows the measured link waveforms at a low supply voltage with the active clamping disconnected. A large overshoot of the bus voltage is observed for one resonant cycle due to the decrease of the inverter DC current. The voltage overshoot must be limited in practice to avoid endangering the inverter devices, and this is accomplished using the active clamping.

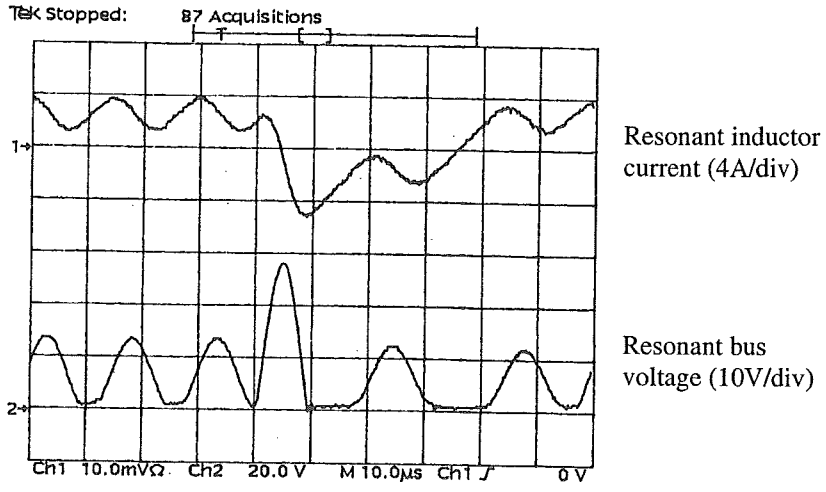


Figure 8.7. Link waveforms of the resonant inverter under a motor load with the active clamping disconnected.

8.2.3 Motoring Operation

After successful operation of the resonant inverter with the motor unloaded at full supply voltage, the motor was then loaded by successively adding weights to the rope up to about 6.9kg. With this load the induction motor delivered an active power of 2.2kW with a phase current of 20.5A rms. The experimental motor current could be varied by a large amount by lifting or dropping the weights suspended on the rope, for example, from 11A rms with the motor unloaded to 20.5A rms with the motor fully loaded. During this large change of the motor current the DC link remained resonating, and the clamping voltage was virtually constant with only a few volts variation.

The resonant inverter was extensively tested under full load conditions for different fundamental frequencies of 30Hz, 50Hz and 70Hz and different PWM switching frequencies from 4kHz to 15kHz. The designed resonant inverter and the link control circuit operated successfully under all these test conditions, except that at some distinct PWM switching frequencies the synchronized PWM scheme would produce low frequency harmonics in motor current. This issue is discussed in the next chapter.

Figures 8.8 and 8.9 show the measured waveforms of the resonant inverter operated with the induction motor fully loaded. For this test, the fundamental frequency was 50Hz, the PWM switching frequency was set to 10.36kHz, and the clamping voltage was set to 440V. Shown in Figure 8.8 are the resonant inductor current and the bus voltage waveforms. The resonant inductor current was measured using a Tektronix TDS 540 digital oscilloscope connected with a Tektronix AM503 current probe and an A503A amplifier. Under this rated load conditions the rms current in the resonant inductor is 21.6A and the peak current is 54A. The peak bus voltage is 468V.

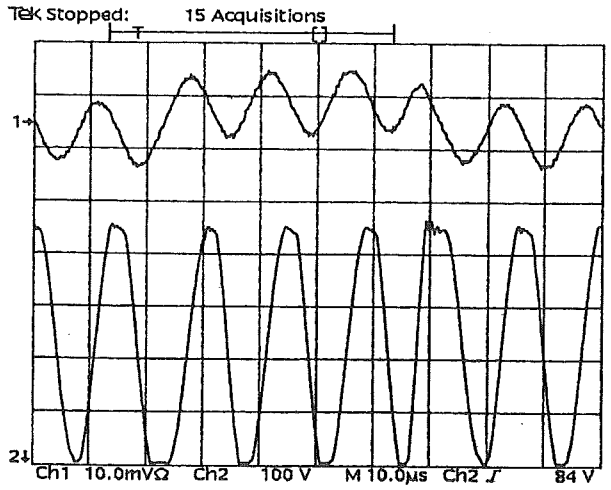


Figure 8.8. Link waveforms of the resonant inverter with the motor fully loaded.

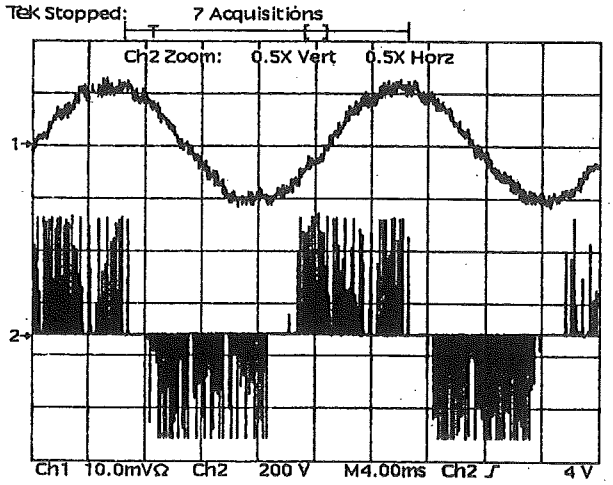


Figure 8.9. Output waveforms of the resonant inverter with the motor fully loaded.

The waveforms shown in Figure 8.9 are the output phase current and line-to-line voltage. Current ripple appears in the motor current due to a low inductance in the motor, in contrast to the clean sinusoidal wave in Figure 8.3 measured from the inductive load tests.

Figure 8.10 confirms the operation of the circuit for predicting the inverter DC current. The upper trace is the predicted signal of the inverter DC current measured from the output of the multiplexer (see Figure 6.3), and it is highly fluctuating with the switching of the inverter devices. The lower trace is the resonant inductor current, which is oscillating with the predicted inverter DC current as a reference. A close

examination of these two waveforms reveals that the predicted inverter DC current changes a little earlier than the inductor current. It is also noticed that the assumption made in Section 2.1.2 that the inverter DC current is constant during one resonant cycle appears to be true by looking at the measurements in Figure 8.10. The measurement of the actual inverter DC current is not available due to the physical layout of the prototype resonant inverter.

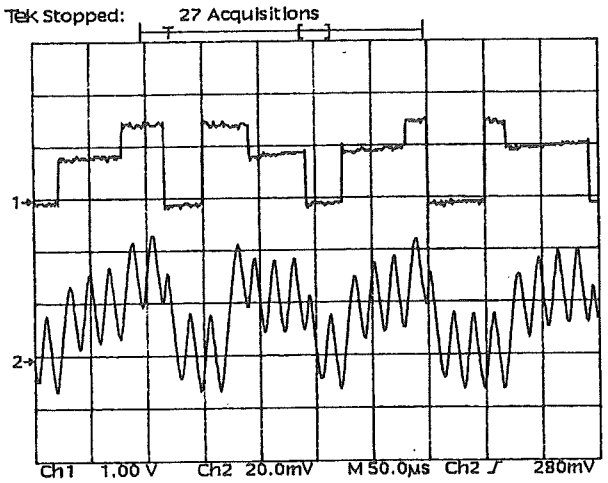


Figure 8.10. Waveforms confirming the inverter DC current prediction scheme.

8.2.4 Regenerating Operation

An electric vehicle application requires frequent regeneration, where energy is fed back to the battery bank through the motor to maximize the usage of battery energy. The resonant DC link inverter was tested in such regenerative circumstances to confirm the capability of bidirectional power flow.

A PDL motor speed control board (Microdrive-3) was used for the regeneration tests. Its programmable features associated with the regeneration control of the motor include: user defined deceleration rate, minimum and maximum frequency settings, supply voltage clamp by reducing the deceleration rate in regenerating mode, and motor current limit [PDL Manual, 2000]. Six PWM switching signals were taken out from the PDL control board, dead time control was added in via a FPGA logic circuitry, then connected to the resonant link control circuit. A "START" command from an output relay on the PDL control board was directly connected to the link control circuit to initiate the link resonance.

The experimental arrangement with the PDL control board was first tested with the motor operating in motoring mode to ensure proper operation. The regeneration tests started with a low deceleration rate of 1Hz/s, slowing the motor down from 70Hz to 30Hz, then the regeneration tests with fast deceleration rates of 5Hz/s and 10Hz/s were carried out.

The experimental results illustrating mode changeover from motoring to regenerating are shown in Figure 8.11. For this test, the induction motor was unloaded, and the resonant inverter was operated at a low supply voltage of 37V. To obtain regeneration the fundamental frequency command of the inverter was reduced from 70Hz to 30Hz at a deceleration rate of 10Hz/s.

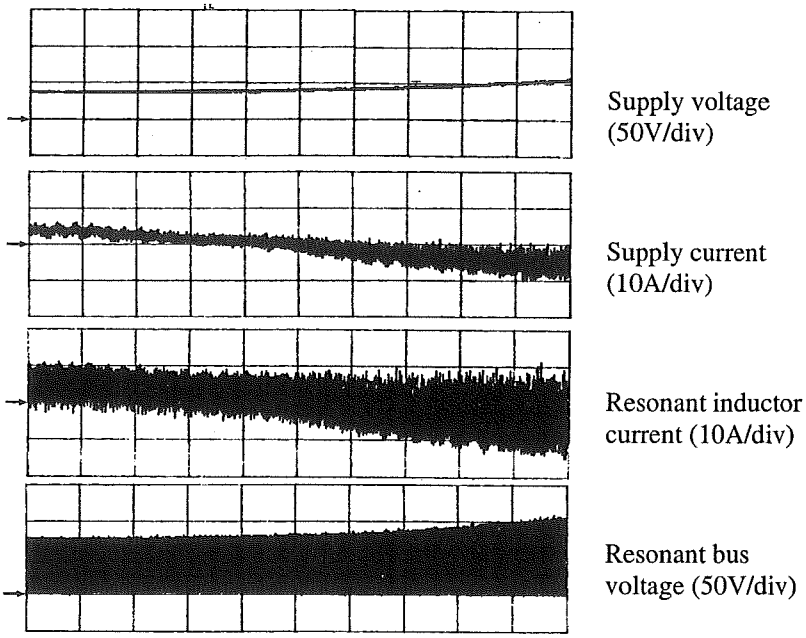


Figure 8.11. Inverter waveforms during the mode changeover from motoring to regenerating (time scale 40ms/div).

As shown in Figure 8.11, shortly after the deceleration of the induction motor, the supply current reverses and goes negative, and it is blocked by the diode rectifier of the DC supply and hence causes the supply voltage to increase. With the increase of the supply voltage the amplitude of the resonant pulses of the bus voltage increases. The resonant inductor current resonates around a positive inverter DC current in motoring mode, following a reversal of power flow the inductor current resonates

around a negative inverter DC current. The DC link remains resonating during the mode changeover from motoring to regenerating.

Figure 8.12 shows an expanded view of the resonant inductor current and the bus voltage waveforms in the regenerating mode. It is clear that the regenerated energy is fed back to the DC supply through the resonant link instead of accumulating in the resonant capacitor. As it can be seen that the average value of the resonant inductor current is negative and the bus voltage has stable resonant pulses implying that no energy is accumulated in the resonant link during the regeneration.

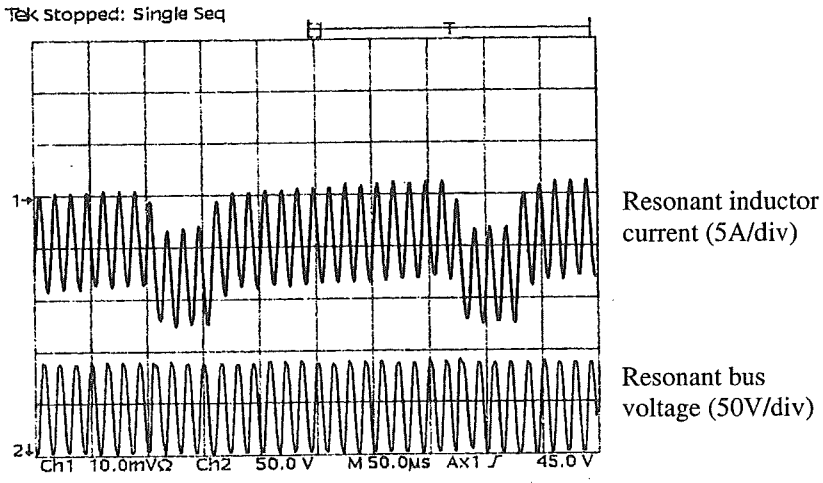


Figure 8.12. Link waveforms in the regenerating mode.

Due to the experimental setup, consisting of the uncontrolled rectifier operated from the AC mains, the regeneration tests at full supply voltage were not performed, since the resulting rise in the supply voltage could damage the components of the resonant inverter. It is believed that with a battery source the prototype resonant inverter can operate successfully in the regenerating mode at full supply voltage.

This unique feature of the resonant DC link inverter being capable of operating in both motoring and regenerating modes with zero voltage switching makes it suitable for the electric vehicle application as it allows a better utilization of battery energy.

8.3 Summary

This chapter has described the operational tests of the prototype resonant DC link inverter under load conditions. Successful operation of the resonant DC link inverter driving an induction motor of 2.2kW has been demonstrated. The measured resonant frequency is about 70kHz under full load conditions, and the measured peak bus voltage is 468V throughout the tests, ensuring an adequate margin for 600V IGBTs. The designed resonant link control circuit functions satisfactorily to maintain the link resonance under the load conditions. The operation of the inverter DC current prediction scheme has been experimentally verified. The regeneration tests have confirmed that the resonant DC link inverter is capable of bidirectional power flow. In the next chapter, a performance evaluation of the prototype resonant DC link inverter is presented.

CHAPTER 9

PERFORMANCE EVALUATION

This chapter presents an evaluation of the performance of the prototype resonant DC link inverter. Here the term performance encompasses power losses and total harmonic distortion (THD) of the motor current. A thermal method, using a thermal box to measure the total losses in the resonant DC link inverter, is described. Power losses in the resonant DC link inverter and hard switching inverter are compared with a variable PWM switching frequency and a variable load current. The spectral characteristic of the synchronized PWM scheme is investigated. THD measurements of the motor current in the resonant DC link inverter and hard switching inverter are presented.

9.1 Loss Measurements

Generally two approaches may be considered for power loss measurement: an electrical method and a thermal method. An electrical method is based on calculating the integral of the product of the current and voltage of a component. It is obvious that any error in the current and voltage waveforms leads an error in the power calculated. The main errors are from [Perret, 1992]:

- nonlinearity of A/D converter of internal amplifier;
- bandwidth limitations of current and voltage probes;
- current and voltage delay time;
- synchronous noise.

For the task of measuring the total losses in the resonant inverter, an electrical method was first attempted. The total power losses were obtained as the difference between the power measured at the DC input and the power measured at the three-phase AC output. Unfortunately, this method gave unreasonable results with all of the

instruments available. The main reason is that the total losses in the inverter are only a few percent of the total power, thus they can be very easily masked by the large measured input or output power.

A thermal method is limited to an evaluation of the total power losses of a component only during steady state conditions. The component, usually a semiconductor device, is mounted on a dedicated heatsink. By measuring the temperature rise along the heatsink power losses can be obtained with the aid of the calibrated data of the heatsink. In the case of the resonant DC link inverter, it is impractical to mount the resonant inductor onto a heatsink for measuring losses. However for a comparison of the total losses in the resonant DC link inverter and hard switching inverter, losses in the resonant inductor have to be taken into account. It was therefore decided to design a thermal box to contain the whole inverter system for measuring the total inverter losses.

9.1.1 Thermal Box

A cardboard box was modified for the purpose of loss measurement, as shown in Figure 9.1. Each side of the cardboard box was thermally isolated with a polystyrene board to minimize heat loss. The inverter to be tested was enclosed inside the box. To make connections of the inverter system to the DC supply, resonant link control circuit, gate drive power supply and the induction motor, holes were made along the side of the box. Through these holes, cold air is taken in, and circulated with help of a small fan (DC 24V) installed inside the box. The dissipated power from the inverter system including gate drives is absorbed by the circulating air, and evacuated by a fan (AC 230V) installed on the top of the box (not shown in Figure 9.1). Temperature rise of the thermal box above ambient, ΔT_{ba}, was monitored with one thermocouple located inside the box and the another located outside the box.

The thermal box was calibrated by applying single phase AC power to a resistive load enclosed inside the box as a heat source. Power dissipated was measured using a digital AC power meter (Yokogawa type 2503) with ±0.1% accuracy. The temperature rise of the thermal box was measured against power dissipation. The results are plotted in Figure 9.2. As shown, the calibration curve is a straight line with a slope of 25.7W/°C.

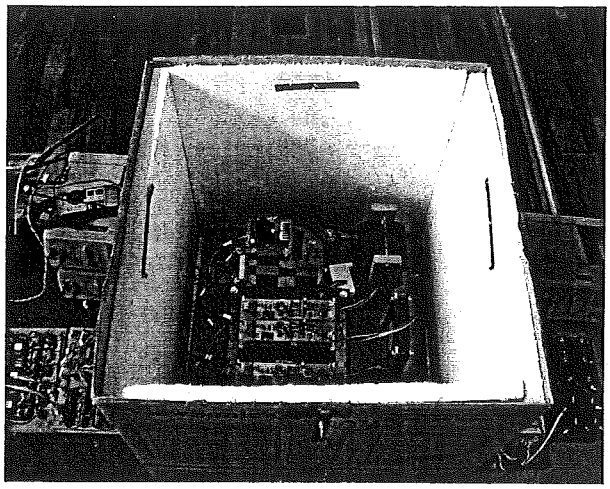


Figure 9.1. A close look of the thermal box.

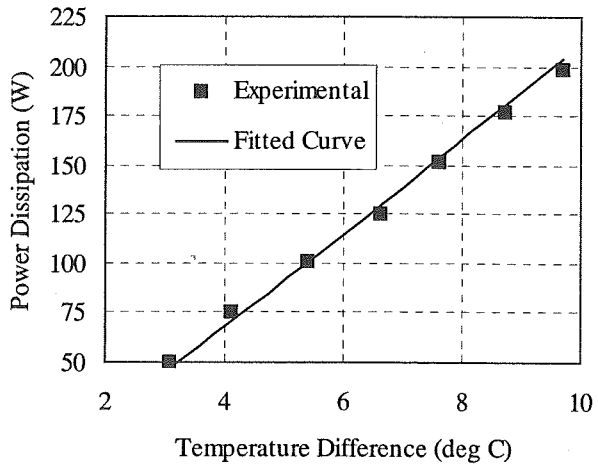


Figure 9.2. Calibration curve of the thermal box.

Using the thermal box and the calibration curve, the total losses in the resonant DC link inverter and hard switching inverter were investigated. Experimental setup for loss measurement was similar to that used for the operational tests shown in Figure 8.4 in the previous chapter, except that the inverter including the gate drives was enclosed in the thermal box.

9.1.2 Switching Losses

In this section, the total losses in the hard switching inverter and the resonant inverter are evaluated with a variable PWM switching frequency and a constant load current. The measured total losses are then compared to investigate the reduction of the switching losses in the resonant DC link inverter.

9.1.2.1 Hard Switching Inverter

The total power losses in the hard switching inverter were measured first for a baseline comparison. As described in Section 5.2, the prototype resonant DC link inverter was configured as a conventional hard switching inverter. The three-phase PWM signal generator was employed to vary the PWM switching frequency. For loss measurements, the supply voltage was 240V DC, the modulation index of the PWM signals was 0.62, and the hard switching inverter was operated to drive the induction motor fully loaded.

The experiment started with a PWM switching frequency of 4kHz, after operation for about one hour, the temperature of the thermal box became stable, and the temperature rise above ambient, ΔT_{ba}, was recorded. The switching frequency was then increased up to 14kHz in steps of 2kHz. Each subsequent measurement was taken after a half an hour settling time. The measured results are plotted in Figure 9.3.

In Figure 9.3, the measured power losses, P_{meas}, were determined from the measured temperature rise at each PWM switching frequency with the calibration curve of the thermal box. The calculated losses, P_{calc}, were obtained using the computer program (Appendix B) based on the actual measurements of the PWM switching frequency, load current and supply voltage. Note that here the calculated power losses also include gate drive losses. It was measured that each gate drive has losses of 1.8 W for normal IGBT operation. Therefore there are additional losses of 10.8W from gate drives for the hard switching inverter.

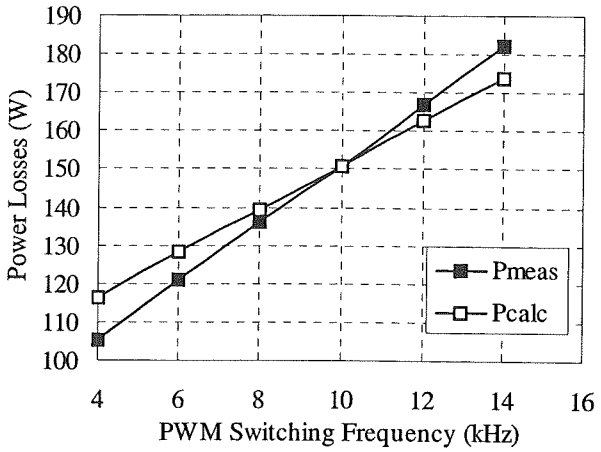


Figure 9.3. Total losses in the HSI versus PWM switching frequency.

As expected, the total losses in the hard switching inverter increase linearly with the PWM switching frequency for a constant load current. The total power losses are in a range of 105W to 182W for a PWM switching frequency range from 4kHz to 14kHz under this specific load condition. In addition, Figure 9.3 indicates reasonably good agreement between P_{meas} and P_{calc} in that the maximum deviation for the measurements is less than 10%. The small discrepancy is due to the accuracy of the IGBT model adopted for calculating the switching losses under the hard switching condition. The calculated power losses, P_{calc}, are found to be very sensitive to the values of switching energy, E_{on} and E_{off}, obtained from the data sheets. Different values of E_{on} and E_{off} give different slopes at which the total power losses increase with the increase of the PWM switching frequency.

The measured total losses represent the combined losses of conduction losses, switching losses, and gate drive losses. Assuming that conduction losses and gate drive losses are unchanged with the increase of the PWM switching frequency, and that the switching losses are in a linear relationship to the PWM switching frequency, then the conduction losses and switching losses can be obtained separately as given in Table 9.1 by extrapolating the measured data [Berringer, 1995]. From Table 9.1, it is clear that the total losses in the hard switching inverter are dominated by the conduction losses at the PWM switching frequency of 4kHz. However, at the PWM switching frequencies above 10kHz, the switching losses become a dominant part of

the total losses under this specific motor load. The inverter efficiency degrades from 95.6% at 4kHz to 92.1% at 14kHz.

Table 9.1 Conduction and Switching Losses in the HSI

Switching frequency (kHz)	Conduction losses (W)	Switching losses (W)
4	64	30
6	64	46
8	64	61
10	64	76
12	64	91
14	64	106

9.1.2.2 Resonant DC Link Inverter

Loss measurements for the resonant DC link inverter were conducted at several PWM switching frequencies under the same load conditions as the hard switching inverter. For all measurements the supply voltage was 240V DC, and the clamping voltage was 440V. To control the output of the resonant inverter the synchronized PWM scheme with the modulation index of 0.62 was applied. The experimental results are given in Figure 9.4.

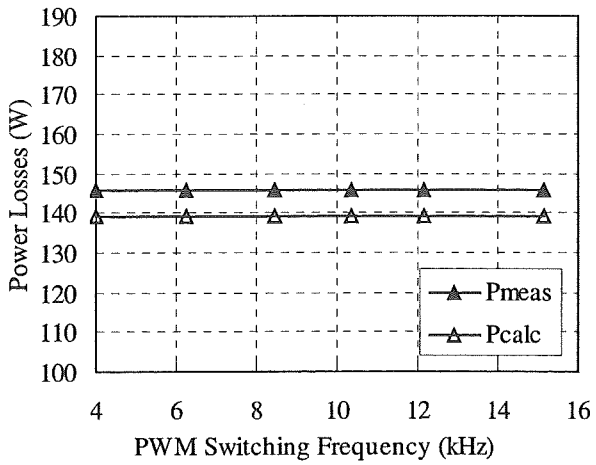


Figure 9.4. Total losses in the ACRLI versus PWM switching frequency.

The measured total power losses in Figure 9.4, P_{meas}, were determined from the measured temperature rise at each PWM switching frequency with the calibration curve of the thermal box. It should be pointed that the PWM switching frequencies at which the power losses in the resonant inverter were measured were not exactly same as in the case of the hard switching inverter, the reason is explained later in this chapter. The calculated losses, P_{calc}, were obtained using the computer program (Appendix B). The calculated power losses, P_{calc}, include losses of 12.6W from seven gate drives.

From Figure 9.4, it can be seen that the measured total losses in the resonant DC link inverter are 146W with the motor fully loaded, and remain constant with the increase of the PWM switching frequency. This strongly demonstrates that zero voltage switching in the resonant DC link inverter decouples the device losses from the PWM switching frequency. As explained before (Section 4.3.2), in the resonant DC link inverter the switching frequency of the main devices depends mainly on the resonant frequency, and the average switching frequency of the main devices equals half the resonant frequency. Thus changing the PWM switching frequency in the resonant inverter does not change the switching frequency of the main devices. This is contrary to the hard switching inverter where the PWM switching frequency is exactly the switching frequency of the inverter devices. Therefore the total losses in the resonant DC link inverter are constant with the increase of the PWM switching frequency.

The agreement between P_{meas} and P_{calc} is considered to be quite reasonable since the difference is only 7W, which may be caused by the calculation models and the measurement errors. The validity of the Equations 4.17 to 4.25 for calculating the power losses in the resonant DC link inverter is verified.

9.1.2.3 Comparison of the ACRLI and HSI Losses

The measured losses in the hard switching inverter and resonant inverter are compared in Figure 9.5. The resonant inverter shows a noticeable loss reduction at the PWM switching frequencies above 10kHz. Looking at the measured losses at 14kHz for the HSI and 15kHz for the ACRLI, the resonant inverter has a power

saving of 36W. That is about 20% of the total losses in the hard switching inverter operated at 14kHz. The reduction of the total power losses in the resonant inverter is attributed to the significantly reduced switching losses of the main devices under the zero voltage switching conditions.

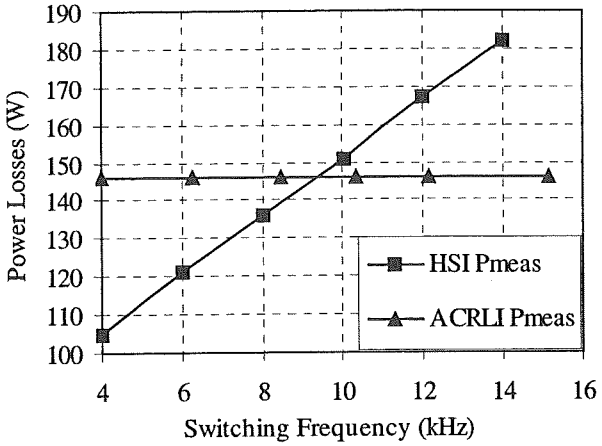


Figure 9.5. A comparison of the measured total losses in the HSI and ACRLI versus the PWM switching frequency.

Bearing in mind that low loss switching of the inverter stage in the resonant inverter is accomplished at expense of the link losses. As measured from the resonant link tests in Chapter 7, power losses of 47W are typically incurred in the resonant link to maintain resonant operation at full supply voltage under no-load conditions. Therefore, it can be said that the switching loss of 83W out of 106W in the hard switching inverter operated at 14kHz (Table 9.1) have been eliminated, that is an elimination of the 78% switching losses in the main devices by the soft switching compared to the hard switching. However at low PWM switching frequencies, the resonant inverter is less efficient because that the resonant link losses are even larger than the switching losses eliminated in the main devices.

9.1.3 Conduction Losses

With substantially reduced switching losses, the total losses in the resonant inverter are mainly made up of the conduction losses of the main devices and the losses in the resonant link, and they are all dependent on load conditions. In this section, the total power losses in the hard switching inverter and resonant inverter are evaluated for

several load currents at a constant PWM switching frequency. The measured results are then compared to investigate the dependency of losses in the resonant inverter on load current.

The total losses in the hard switching inverter were measured for several motor currents at a constant switching frequency of 14kHz. Motor current was varied by varying weights on the rope/drum braking system. For all measurements the supply voltage was 240V DC, and the modulation index was 0.62. The motor current was varied from 14.9A rms for the output power of 1.55kW to 20.5A rms for the output power of 2.2kW, while power factor was changed slightly from 0.73 to 0.83 with the motor current. The measured results are given in Figure 9.6. Power losses in the resonant DC link inverter were evaluated for several motor currents at a constant PWM switching frequency of 15kHz. The experimental results are also plotted in Figure 9.6.

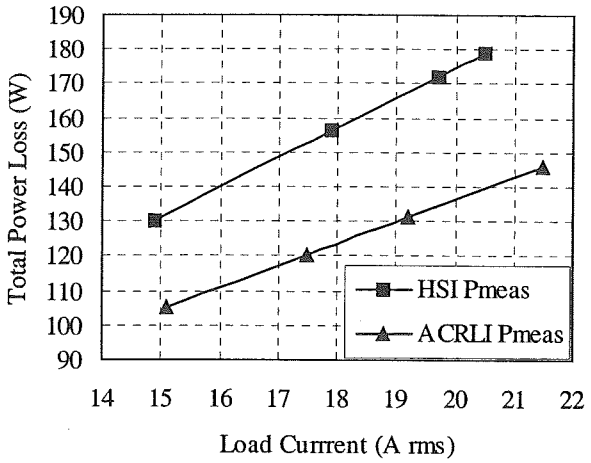


Figure 9.6. A comparison of the total losses in the HSI and ACRLI versus load current.

The measured total losses in the hard switching inverter include the conduction losses, switching losses and the gate drive losses. For a constant PWM switching frequency, the switching losses are proportional to the load current. Given a fixed modulation index and a virtually constant power factor the conduction losses are also proportional to the load current. As it can be seen from Figure 9.6 that the total losses in the hard switching inverter increase linearly with the load current for a constant PWM

switching frequency. The slope at which the total losses increase with the load current is determined by the electrical characteristics of the main devices

The total losses in the resonant inverter increase linearly with load current as shown in Figure 9.6. As mentioned before that the switching losses are greatly reduced in the resonant inverter, hence, conduction losses of inverter stage become the main power losses. Furthermore, under the same load conditions and for the same inverter devices, the conduction losses in the resonant inverter can be considered to be same as in the hard switching inverter since the main devices are minimally involved with the link resonance [Dahono, 1995].

Under load conditions, the inverter DC current flows through the resonant inductor and also marginally increases the peak current in the clamp device. It has been analyzed that the load dependent losses in the resonant link are insignificant given a high quality factor of the resonant inductor. It is noticed from Figure 9.6 that the slope at which the total losses increase with the load current in the resonant inverter is lower than that in the hard switching inverter. This justifies that there is only a small increase of the losses in the resonant link with the load current. In fact, when the resonant inverter delivers output power of 2.2kW, the average inverter DC current flowing through the resonant inductor is only about 10A, causing only a few watts of losses in the ESR (49mΩ, for quality factor of 190 as measured) of resonant inductor. The additional losses in the clamp device due to the inverter DC current are also very small with a high clamping ratio of 1.83.

It is seen from Figure 9.6 that the total losses in the resonant inverter are greatly reduced compared to the hard switching inverter as a result of the low switching losses in the main devices. With low switching losses, the device utilization in the resonant inverter may be improved by increasing the forward current while maintaining the same total losses as in the hard switching inverter [Divan, 1997]. For example, the resonant inverter delivering a load current of 21.5A rms has the same total losses as in the hard switching inverter delivering a load current of 16.5A rms.

9.2 THD Measurements

In the conventional hard switching inverters, a sinusoidal PWM technique is most commonly applied to control the inverter output. The advantages of the sinusoidal PWM technique include real-time control, linear operation, good transient response and a constant switching frequency of the main devices [Habetler, 1991]. In the resonant DC link inverter the bus voltage is periodic, the interval between allowed switching instants is constrained by the resonant frequency, and the inverter output must be synthesized with the discrete pulses of the bus voltage. This characteristic means that the well-established sinusoidal PWM technique is not suitable. In this project, the synchronized PWM scheme described in Section 6.1.4 was implemented for the output control of the resonant inverter with the intention of preserving the advantages of the sinusoidal PWM technique and achieving zero voltage switching of the main devices. This section investigates the spectral characteristic of the synchronized PWM scheme, and presents the THD measurements of the motor current

9.2.1 Synchronized PWM Scheme

The synchronized PWM scheme is illustrated in Figure 9.7. A sinusoidal PWM signal, S_b, is synchronized to the resonant bus voltage by a sample and hold clocked at the resonant frequency f_r. The output signal, S_a, of the sample and hold is composed of a sequence of pulses with a period of $1/f_r$.

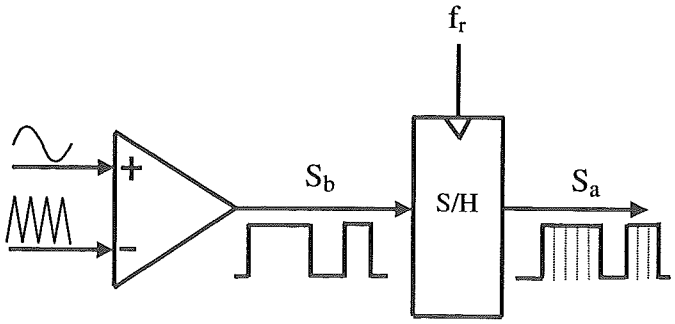


Figure 9.7. The synchronized PWM scheme.

As discussed in Section 2.2.3, the resonant frequency varies with the inverter DC current due to the modulation of the inverter, this results in a random sampling of the sinusoidal PWM signal S_b, therefore, the well-defined switching pattern of the sinusoidal PWM is inevitably altered. First, the pulse width after synchronization has to be multiples of the resonant pulse width, this means that in the power circuit the switching of the main devices (on or off) has to be made at zero crossing of the bus voltage. This constraint of switching instant creates energy at frequencies substantially below the resonant link frequency [Venkataramanan, 1993]. Secondly, a narrow pulse or a train of narrow pulses of signal S_b may not be transferred to the output signal S_a by the sampling process, this event happens in a very low frequency manner, and may cause a low frequency distortion in motor current. Furthermore, there is an increased probability of missing a train of pulses for a high PWM switching frequency, especially, when the PWM switching frequency happens to be the 1/N of the resonant frequency (N is an integer).

Figure 9.8a shows the spectrum of the resonant bus voltage under a no-load condition, with the link frequency a constant of 70kHz. Since the bus voltage is a clamped sinusoid, and there is a bus shorting time between the pulses, there are distinct frequency components at multiples of the link frequency. Under load conditions, the pulse width, bus shorting time, and the active clamping time of the bus voltage vary with the inverter DC current, a series of low level components appear at frequencies around the resonant frequency as shown in Figure 9.8b.

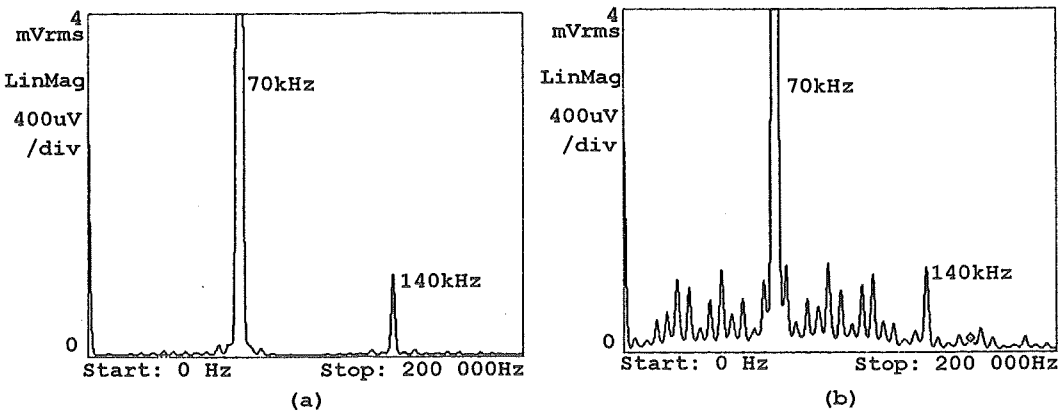
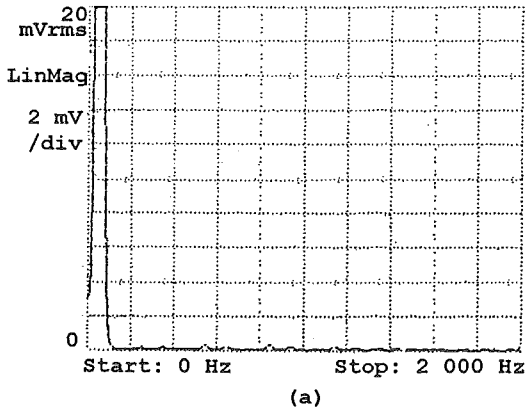
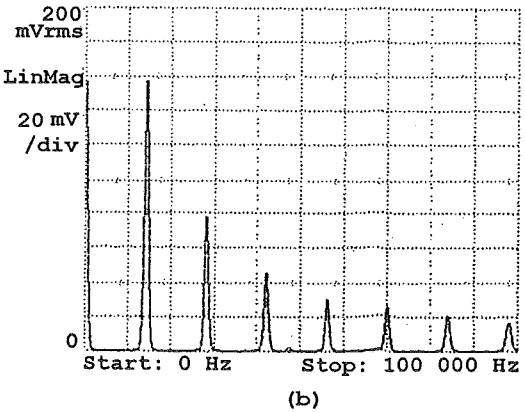


Figure 9.8. Spectra of the bus voltage. (a) no-load, (b) with a load.

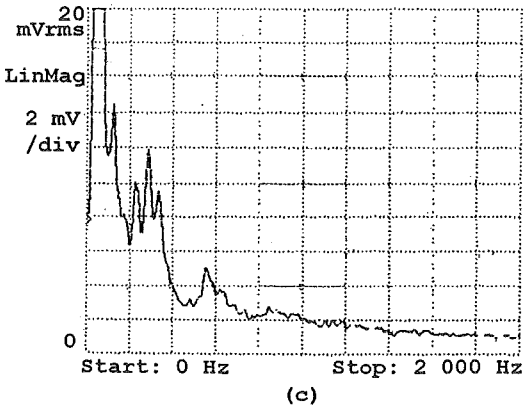
Figure 9.9 shows the spectra of the sinusoidal PWM signal and the synchronized PWM signal at a PWM switching frequency of 14kHz. Note that there are no harmonics over a 2kHz frequency band in Figure 9.9a for the sinusoidal PWM signal. In contrast, low frequency components appear over the 2kHz frequency band in Figure 9.9c for the synchronized PWM signal due to the sampling process. Looking at Figure 9.9b for the sinusoidal PWM signal, the harmonics occur only at side bands around the multiples of the PWM switching frequency of 14kHz. However, after the sampling process, the harmonic components contained originally in the sinusoidal PWM signal appear at side bands of the resonant frequency and its multiples according to the sample theory [Haykin, 1983]. It is evident that the 5^{th} harmonic (70kHz component) disappears in Figure 9.9d as a consequence of the sampling process.



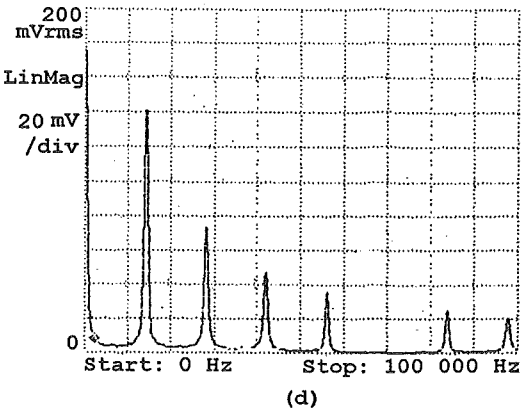
(a) Sinusoidal PWM over 2kHz bandwidth



(b) Sinusoidal PWM over 100kHz bandwidth



(c) Synchronized PWM over 2kHz bandwidth

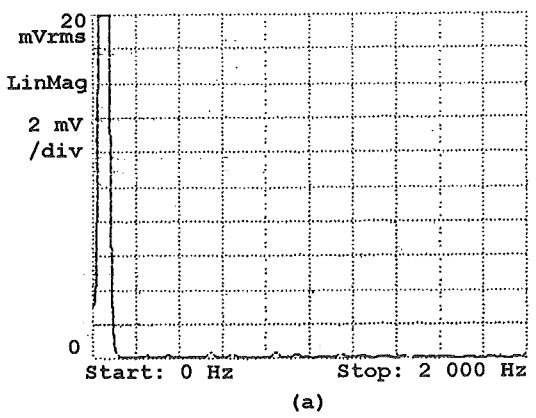


(d) Synchronized PWM over 100kHz bandwidth

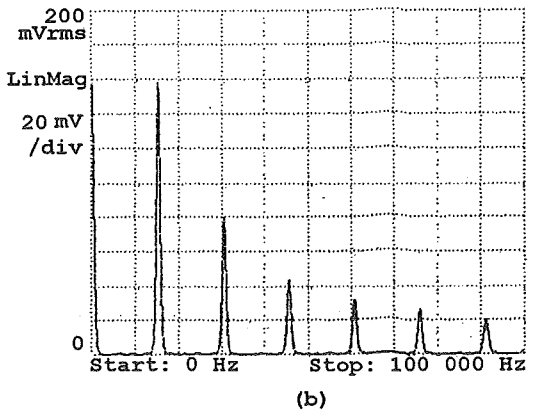
Figure 9.9. Spectra of the sinusoidal PWM signal and the synchronized PWM signal at a PWM switching frequency of 14kHz.

Figure 9.10 shows this effect more clearly with the spectra of the sinusoidal PWM signal and the synchronized PWM signal at a PWM switching frequency of 15kHz. The spectral contents concentrated at the multiples of 15kHz in Figure 9.10b for the sinusoidal PWM signal now spread out over a wide frequency range in Figure 9.10d.

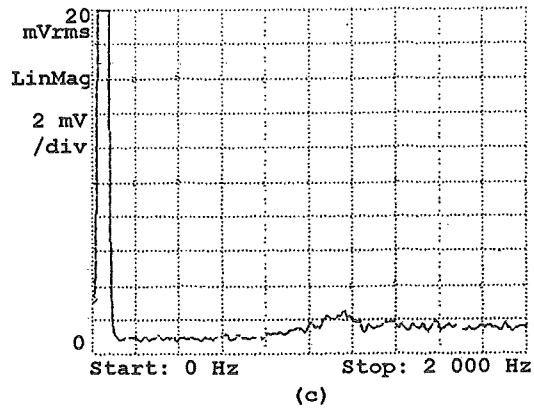
Comparing the measurements in Figure 9.10c and Figure 9.9c, it is important to find that the amplitudes of the low frequency components are substantially reduced for the PWM switching frequency of 15kHz, especially over the frequency band below 600Hz. These measured results support the statement that the synchronized PWM scheme may cause low frequency distortion if the PWM switching frequency happens to be 1/N of the resonant frequency as in the case of Figure 9.9c where the PWM switching frequency of 14kHz is exactly a fifth of the resonant frequency of 70kHz.



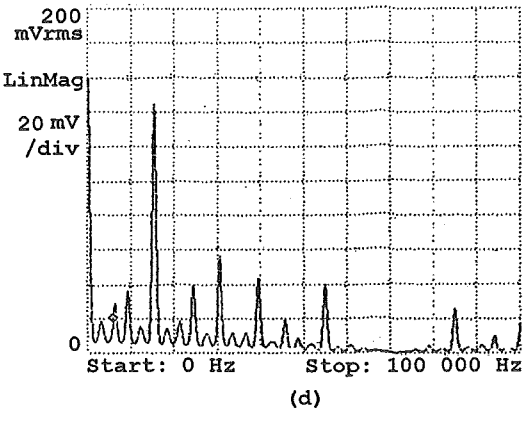
(a) Sinusoidal PWM over 2kHz bandwidth



(b) Sinusoidal PWM over 100kHz bandwidth



(c) Synchronized PWM over 2kHz bandwidth



(d) Synchronized PWM over 100kHz bandwidth

Figure 9.10. Spectra of the sinusoidal PWM signal and the synchronized PWM signal at a PWM switching frequency of 15kHz.

9.2.2 Motor Current THD

The THD (Total Harmonic Distortion) value of the motor current was measured for the hard switching inverter and resonant inverter modulated by the synchronized PWM scheme for a PWM switching frequency range from 4kHz to 15kHz. For all measurements, the induction motor was operated under full load. THD measurements were performed using an HP3561 spectrum analyzer. The measured THD value includes up to the 20^{th} harmonics of the fundamental frequency of 50Hz. The measured results are given in Figure 9.11.

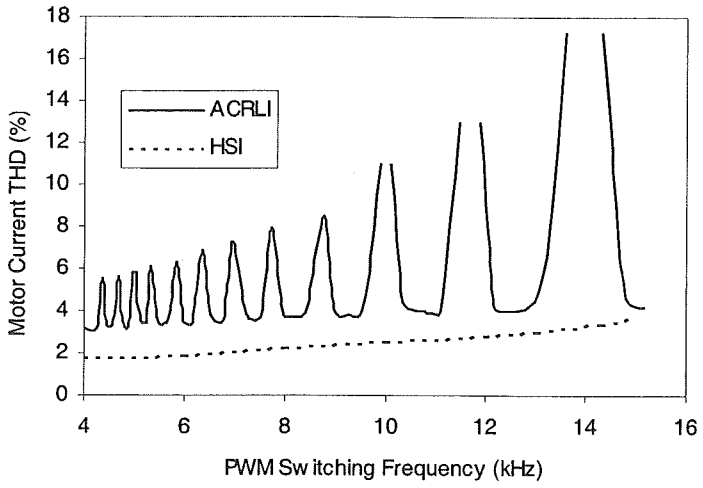


Figure 9.11. Measured THD of the motor current in the HSI and ACRLI versus the PWM switching frequency.

As shown in Figure 9.11, at some distinct PWM switching frequencies, the resonant DC link inverter modulated by the synchronized PWM scheme causes a much higher THD value of the motor current compared to the hard switching inverter modulated by the conventional PWM technique. These PWM switching frequencies are 14kHz, 11.67kHz and down to 4.38kHz. In particular, at the PWM switching frequencies of 10kHz, 11.67kHz and 14kHz, THD measurements of the resonant inverter were not available because that the severely distorted motor current tripped the protection circuit and shut down the inverter operation.

Generally the THD value of the motor current in the resonant DC link inverter is in the range of 3-4% except at the PWM frequencies in the vicinity of those distinct frequency points. It is very comparable to the THD value of the motor current in the

hard switching inverter, which is in the range of 2%-3%. Therefore, the synchronized PWM scheme is workable.

The PWM switching frequency at which the resonant inverter operates should be carefully selected to avoid low frequency distortion of the motor current. The experimental results show that at the PWM switching frequencies between 12kHz and 13kHz, the resonant inverter has a similar THD value of the motor current to the hard switching inverter, but it is more efficient than the hard switching inverter operating at the same PWM frequency.

Finally, it was found during the tests of the resonant inverter that the audible noise generated by the induction motor was reduced at certain PWM switching frequencies, the annoying whine becoming a soft hiss. The acoustic noise reduction is attributed to the fact that the energy spectrum for the synchronized PWM scheme is spread out due to the random sampling of the switching pattern [Habetler, 1991].

9.3 Summary

In this chapter, a detailed investigation of power losses in the resonant DC link inverter and hard switching inverter has been presented. Loss measurements show that the power losses in the resonant inverter remain constant with an increase of PWM switching frequency, and that under the same load conditions for the same inverter devices the resonant inverter is more efficient than the hard switching inverter operating at the PWM frequencies above 10kHz. Typically, the resonant inverter has a 78% reduction of the switching losses in the main devices and a 20% reduction of the total losses in comparison to the hard switching inverter operating at a PWM frequency of 14kHz. The losses in the resonant link are not very dependent on the load current. The major load current dependent losses are the conduction losses in the main devices. Using a thermal box to measure the total losses in the resonant inverter has been proved to be a successful method. THD measurements show that the synchronized PWM scheme is workable, and that the THD value of the motor current in the resonant inverter is in a range of 3% to 4%. However, at some distinct PWM frequencies, this scheme produces low frequency distortion in the motor current. In

the next chapter a suggestion for future work to improve the resonant inverter control is presented.

CHAPTER 10

FUTURE WORK

In this project the synchronized PWM scheme has been used to modulate the resonant DC link inverter. This scheme allows the sinusoidal PWM signals to be directly interfaced with the resonant link control circuit, and the experimental comparison of the switching losses in the resonant inverter and hard switching inverter to be successfully performed. However, as discussed in Section 9.2.1, this synchronized PWM scheme may produce low frequency distortion in the motor current at some distinct PWM frequencies. Since the harmonic components of the sinusoidal PWM signal are determined by a fixed carrier frequency, after the sampling process, some harmonic components would appear as the low frequency components in the synchronized PWM signal. For example, a sinusoidal PWM signal at approximately 14kHz contains harmonic components with the 5^{th} harmonic being close to 70kHz. The modulation of this with the resonant frequency of 70kHz causes low frequency distortion in the motor current. In addition, using the synchronized PWM scheme the spectral performance of the resonant inverter is pre-determined by the sinusoidal PWM signal and can not be improved over the hard switching inverter.

10.1 Sigma Delta Modulation

Sigma delta modulation ($\Sigma\Delta M$) is probably the modulation strategy most commonly applied to resonant DC link inverters [Finney, 1993]. The block diagram of a sigma delta modulator is shown in Figure 10.1 [Kheraluwala, 1990]. V_r is a sinusoidal reference signal, which determines the output fundamental frequency of the inverter, and V_f is a two-level switching signal applied to a gate drive. In this modulator, the difference between the reference signal and the switching signal is fed to an integrator

to produce an integrated error signal E. This is then fed to a quantizer, and the output of the quantizer depends on the polarity of E. The quantizer output is strobed by a sample and hold clocked at the resonant frequency f_r to generate the switching signal for the inverter.

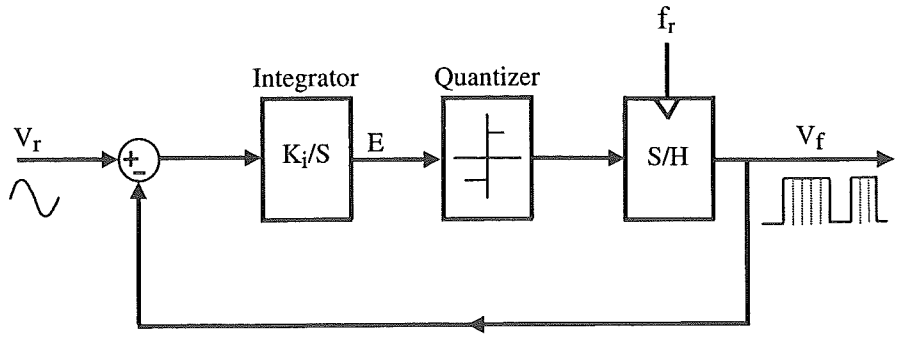


Figure 10.1. Block diagram of a sigma delta modulator.

The spectrum of the switching signal in the sigma delta modulator is mainly determined by the resonant frequency, in contrast to the synchronized PWM scheme (Figure 9.7) where the spectrum is pre-determined by the carrier frequency, and altered due to the sampling process. It has been shown in an application by Kheraluwala that the sigma delta modulator results in virtually no motor current harmonics up to 2kHz, and the harmonic components only appear over a plateau region centered at $f_r/2$ [Kheraluwala, 1990]. Further, it has been found that provided the resonant frequency is 3 to 4 times the PWM switching frequency, a resonant DC link inverter modulated by a sigma delta modulator can realize comparable harmonic levels with a hard switching PWM inverter [Kheraluwala, 1990]. Therefore, it can be expected that the prototype resonant DC link inverter designed for this project would offer an improved spectral performance if the sigma delta modulation strategy were used in the future.

CHAPTER 11

CONCLUSIONS

This thesis has presented the design, implementation, and test results of a resonant DC link inverter for an electric vehicle application. The prototype resonant DC link inverter operates off a nominal supply voltage of 240V DC, and drives a 2.2kW induction motor. The resonant link is composed of a resonant inductor of 20.45μH and a resonant capacitor of 0.234μF, and has a resonant frequency of approximately 70kHz.

Analysis of inverter operation reveals that the difference between the resonant inductor current and the inverter DC current at the beginning of a resonant cycle determines whether the resonant bus voltage will return to zero after the resonant cycle. The analysis also shows that bus overvoltage may occur when the inverter DC current decreases, and that this bus overvoltage can be limited to an acceptable level using active clamping.

Simulations have demonstrated bi-directional operation of a resonant DC link inverter with a three-phase load. It has been found that the additional current stresses on the main devices as a result of resonant operation are minimal. The simulations show that the stray inductance in the resonant inverter causes detrimental oscillations in the bus voltage during the active clamping and bus shorting.

Equations have been developed for calculating the power losses in the resonant DC link inverter. Loss calculations show that the switching losses in the resonant inverter are significantly reduced due to a slow increase of the device voltage during the switching, and that the total losses are very sensitive to the resonant impedance. A

design optimization has been performed to find the optimal values of the link components.

A prototype resonant DC link inverter has been constructed using 50A/600V IGBT modules, with the top and bottom three IGBTs in each module paralleled to obtain the required current rating. By minimizing the interconnection distance between components and incorporating a laminated bus structure into the assembly, the stray inductance in the resonant inverter has been minimized.

A resonant link control circuit has been developed. Using the predicted inverter DC current as a reference, the inductor charging control ensures a proper initial current in the resonant inductor. The predicted signal is obtained using a multiplexer with inputs of the three phase load currents and the switching signals. A synchronized PWM scheme, in which sinusoidal PWM signals are synchronized with the zero crossings of the bus voltage, has been used to modulate the resonant inverter.

The prototype resonant DC link inverter has been tested extensively. Successful operation of the resonant inverter under a rated load has been demonstrated. It has been experimentally confirmed that the resonant DC link inverter is capable of bi-directional power flow. The measured peak bus voltage of 468V gives an adequate margin for 600V IGBTs. The control circuit functions satisfactorily to maintain resonant operation throughout the tests.

Loss measurements show that the power losses in the resonant inverter remain constant with an increase of PWM switching frequency, and that under the same load conditions for the same inverter devices the resonant inverter is more efficient than a hard switching inverter operating at PWM frequencies above 10kHz. Typically, the resonant inverter has a 78% reduction of the switching losses in the main devices and a 20% reduction of the total losses in comparison to the hard switching inverter operating at 14kHz.

THD measurements show that the synchronized PWM scheme could be implemented in an industrial system, and that the typical operating THD value of the motor current is in a range of 3% to 4%. However, at some distinct PWM switching frequencies,

this scheme produces low frequency distortion in the motor current. Future work on this project will allow a sigma delta modulation strategy to be used to improve the spectral performance of the resonant DC link inverter.

Overall this project has shown that a resonant DC link inverter has the advantages of low losses, low acoustic noise, a low dv/dt, a high switching frequency, and snubberless operation. Therefore, the resonant DC link inverter has a promising application to electric vehicle propulsion.

REFERENCES

Berringer Ken, (1995), "Semiconductor Power Loss in AC Inverter," in *Conf. Rec. IEEE-IAS Annu. Meeting*, pp. 882-888.

Bellar Maria D, Wu Tzong-Shiann, Tchamdjou Aristide, Mahdavi Javad, and Ehsani M., (1998), "A Review of Soft-Switched DC-AC Converters," *IEEE Trans. Ind. Applicat.*, vol. 34, pp. 847-860, July/August.

Clemente Steve, (1995), "A Simple Tool for the Selection of IGBTs for Motor Drives and UPSs", in *APEC'95 Rec.*, pp. 755-764.

Chan C. C. and Chau K. T., (1997), " An Overview of Power Electronics in Electric Vehicles" *IEEE Trans. Ind. Electron.*, vol. 44, no. 1, pp. 3-13, February.

Divan Deepakraj M., (1989a), " The Resonant DC Link Converter- A New Concept in Static Power Conversion," *IEEE Trans. Ind. Applicat.*, vol. 25, pp. 317-324, March/April.

Divan Deepakaj M. and Skibinski Gary, (1989b), " Zero-Switching-Loss Inverters for High-Power Applications," *IEEE Trans. Ind. Applicat.*, vol. 25, pp. 634-643, July/August.

Divan Deepakaj M. and Venkataramanan Giri, (1993) " Design Methodologies for Soft Switched Inverters," *IEEE Trans. Ind. Applicat.*, vol. 29, pp. 126-135, January/February.

Divan Deepakaj M. and Wallace Ian, (1997), " New Developments in Resonant DC Link Inverters," in *Conf. Rec. PCC'97-Nagaoka*, pp.311-318.

Dahono P. A., Sato Y., and Kataoka T., (1995), "Analysis of Conduction Losses in Inverters", in *Proceedings of IEE Electric Power Applications*, vol. 1424, pp. 225-2232.

Deshpande Vijay V., and Doradla Seshagiri Rao, (1996), " A New Topology for Parallel Resonant DC Link with Reduced Peak Voltage" *IEEE Trans. Ind. Applicat.*, vol. 32, pp. 301-307, March/April.

Deshpande Vijay V., Doradla Seshagiri Rao, and Divan Deepakaj M., (1997), " A Current-Prediction Scheme for the PRDCL Inverter-Fed Induction Motor Drive," *IEEE Trans. Power Electron.*, vol. 12, pp. 64-70, January.

Finny Stephen J., Green Tim C., and Williams Barry W., (1993), "Spectral Characteristics of Resonant Link Inverters", *IEEE Trans. Power Electron.*, vol. 8, pp. 562-570, October.

Haykin Simon, (1983), *Communication System*, 2nd Edition, John Wiley & Sons.

Habetler Thosmas G. and Divan Deepakraj M., (1991), "Acoustic Noise Reduction in Sinusoidal PWM Drives Using a Randomly Modulated Carrier," *IEEE Trans. Power Electron.*, vol. 6, pp. 356-363, July.

Kheraluwala Mustansir H. and Divan Deepakaj M., (1990) " Delta Modulation Strategies for Resonant Link Inverters," *IEEE Trans. Power Electron.*, vol. 5, pp. 220-228, April.

Kurnia Alexander, Cherradi Hassan, and Divan Deepakaj M., (1995), " Impact of IGBT Behavior on Design Optimization of Soft Switching Inverter Topologies," *IEEE Trans. Ind. Applicat.*, vol. 31, pp. 280-286, March/April.

Kerkman Russel. J., Skibinski Gary L., and Schlegel David W., (1999), "AC Drives: Year 2000 (Y2K) and Beyond", in *APEC'99 Rec.*, pp. 28-39.

Li Xiaoming, (1999), "Design of a Three-Level Inverter For an Electric Vehicle", M.E. Thesis, University of Canterbury, Christchurch, New Zealand.

McLyman Colonel Wm. T., (1988), *Transformer and Inductor Design Handbook,* 2nd Edition, Marcel Dekker, Inc.

Mertens Axel and Divan Deepakaj M, (1990), " A High Frequency Resonant DC Link Inverter Using IGBTs," in *IPEC'90 Rec.*, pp. 152-160.

Mohan Ned, Undeland Tore M., and Robbins William P., (1995), *Power Electronics Converters, Applications, and Design*, 2nd Edition, John Wiley & Sons.

Nielsen Munk, Blaabjerg F., Pedersen J. K., Protiwa F. F. and Apeldoorn O., (1996) "A New Parallel Resonant Converter Link Voltage Control," in *Proceedings of power Electronics, Drives and Energy System for Industrial Growth*, pp. 27-32.

Perret R., Schaeffer Ch., and Farjah E., (1992), "Temperature Evaluation in Power Semiconductor Devices: Measurement techniques for Power Electronics", in *IEE Colloquium on Power Electronics*, pp.101-107.

PDL Electronics Ltd., (2000), *Microvector Series Instruction Manual*, New Zealand.

Siemens, (1991), *Ferrites and Accessories*, Data book, Germany.

Siemens, (1995), *IGBT Modules*, Data book, Germany.

Schulting L., (1992), "A 100kVA Resonant DC Link Inverter with GTOs- Design Considerations and First Practical Experience," in *Conf. Rec. IEEE-IAS Annu. Meeting*, pp. 29-736.

Skibinski G. L. and Divan D. M., (1993a), " Design Methodology and Modeling of Low Inductance Planar Bus Structure", in *Rec. of Fifth European Conference on Power Electronics and Application*, pp.1029-1040.

Skibinski G. L. and D. M. Divan, (1993b), " Design Integration of a 200kW GTO RDCL Converter," in *Conf. Rec. IEEE-IAS Annu. Meeting*, pp.1029-1040.

Suh Duk-Bae, Choi Jong-Woo, and Sul Seung-Ki, (1996), " Voltage Gradient Suppression in Application of Voltage-Fed PWM Inverter to AC Motor Drives—Resonant DC Link Inverter Approach," in *APEC'96 Rec.*, pp.601-606.

Undeland Tore M., Lode Jon, Nilssen Robert, Robbins William P. and Mohan Ned, (1996), "A Single-Pass Design Method for High-Frequency Inductors," *IEEE Industry Applications Magazine*, September/October.

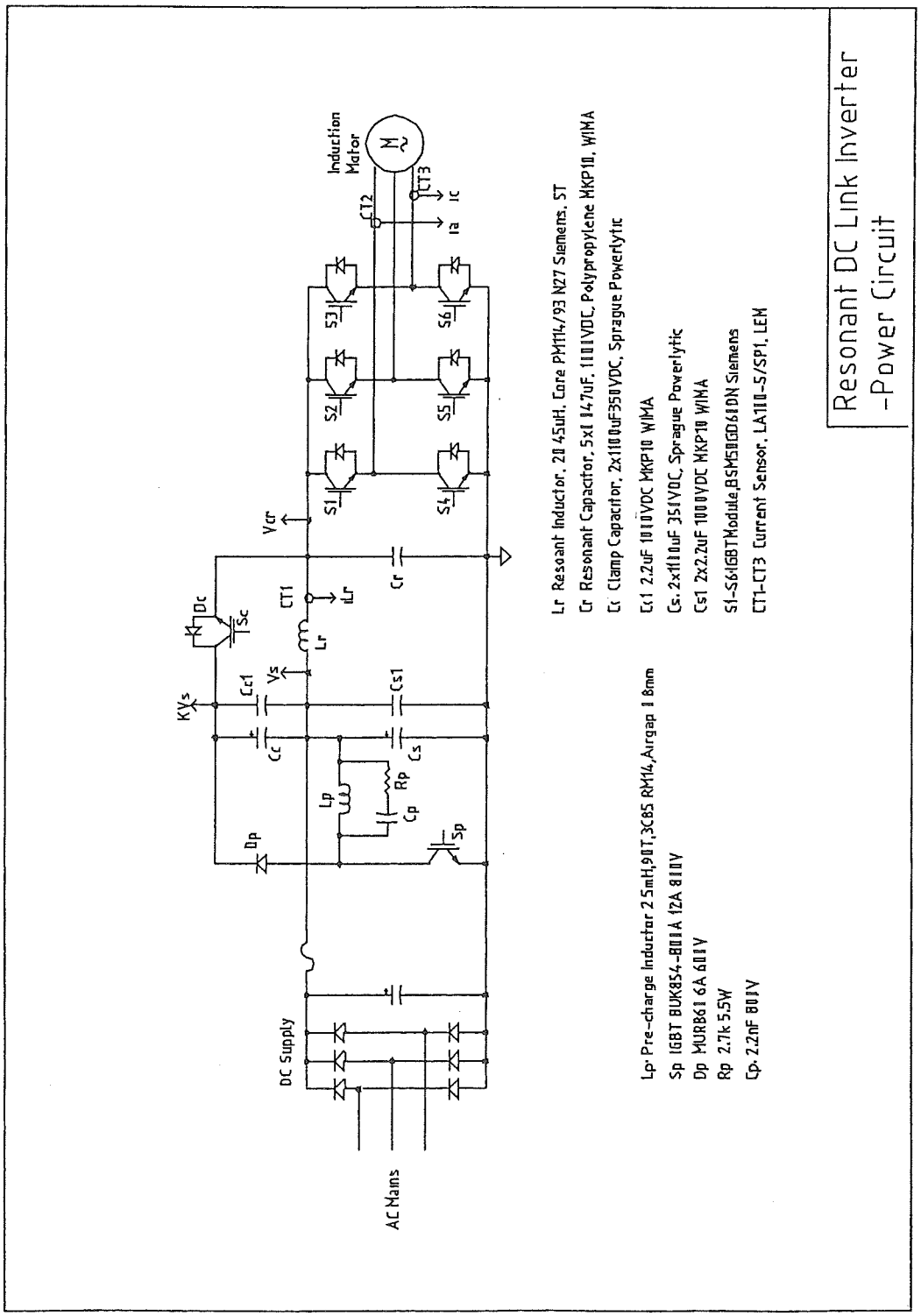
Venkataramanan Giri and Deepakaj M Divan, (1993) " Pulse Width Modulation with Resonant DC Link Converters," *IEEE Trans. Ind. Applicat.*, vol. 29, pp. 113-120, January/February.

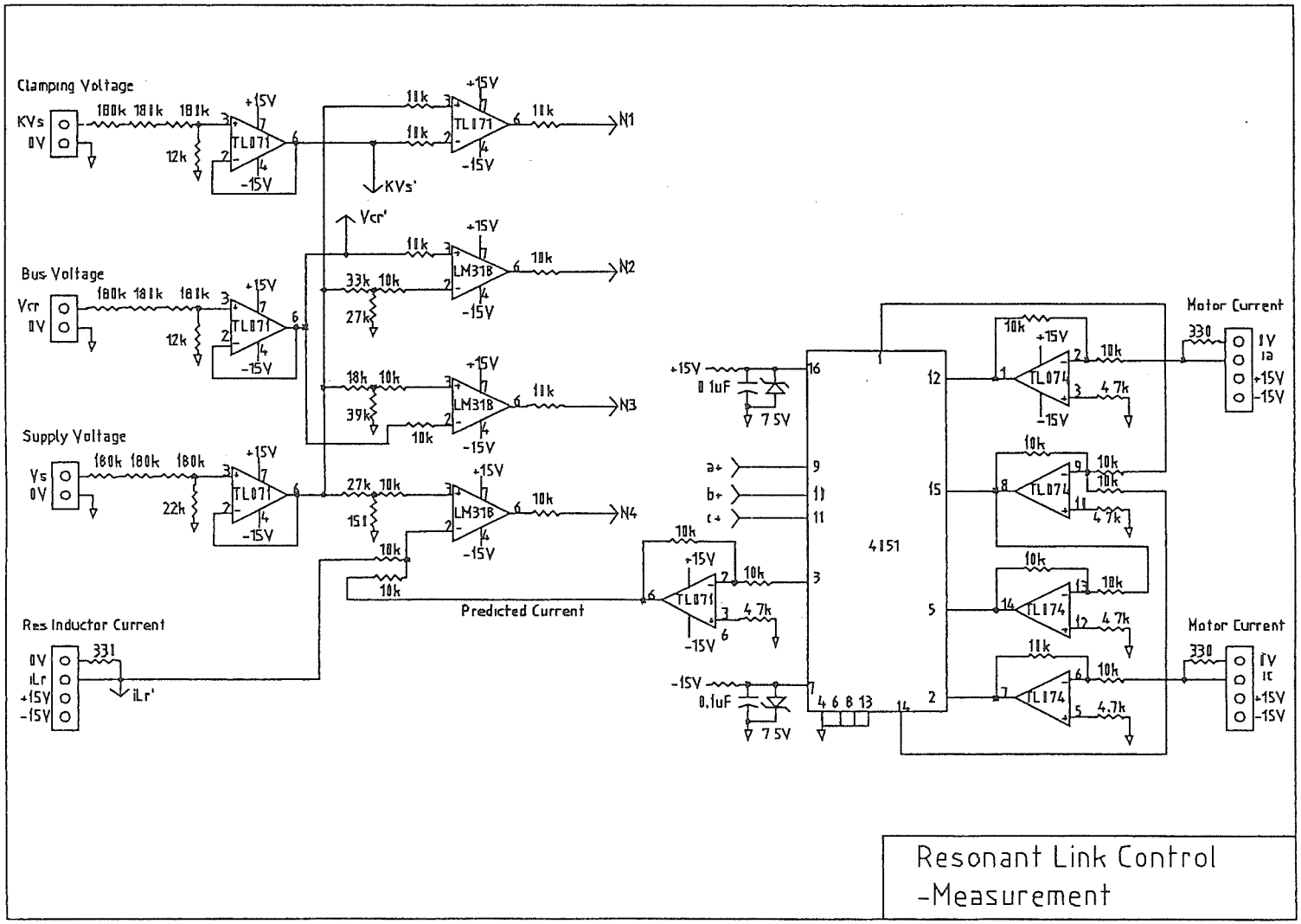
Williams Mark Richard, (1993), "A Controlled Current Inverter for an Electric Vehicle", M.E. Thesis, University of Canterbury, Christchurch, New Zealand.

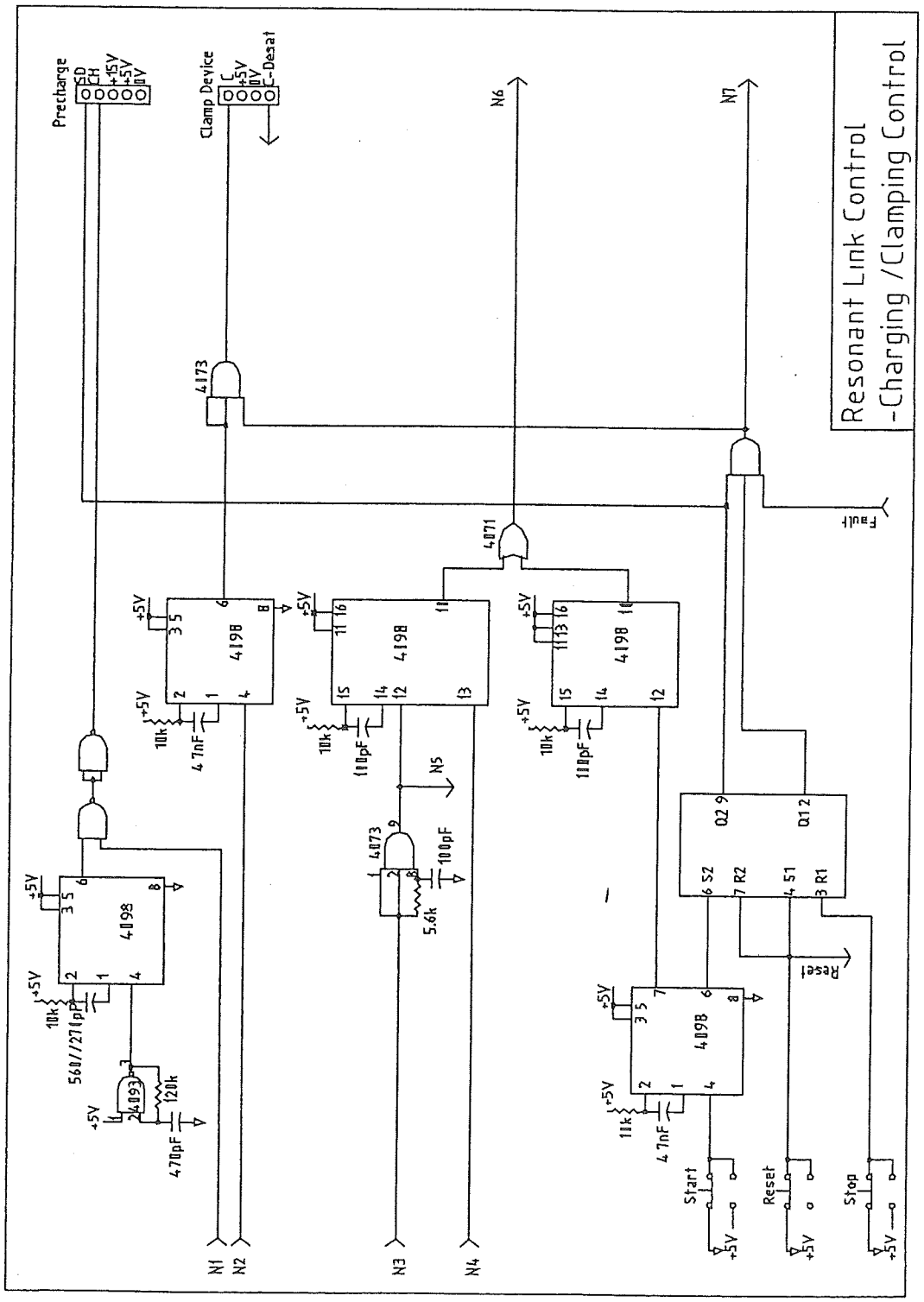
Williams N., (1996), " Metalised Film Capacitor for High Frequency, High Current Applications," in *IEE Colloquium on Capacitor and Inductor for Power Electronics*, pp. 4/1-4/4.

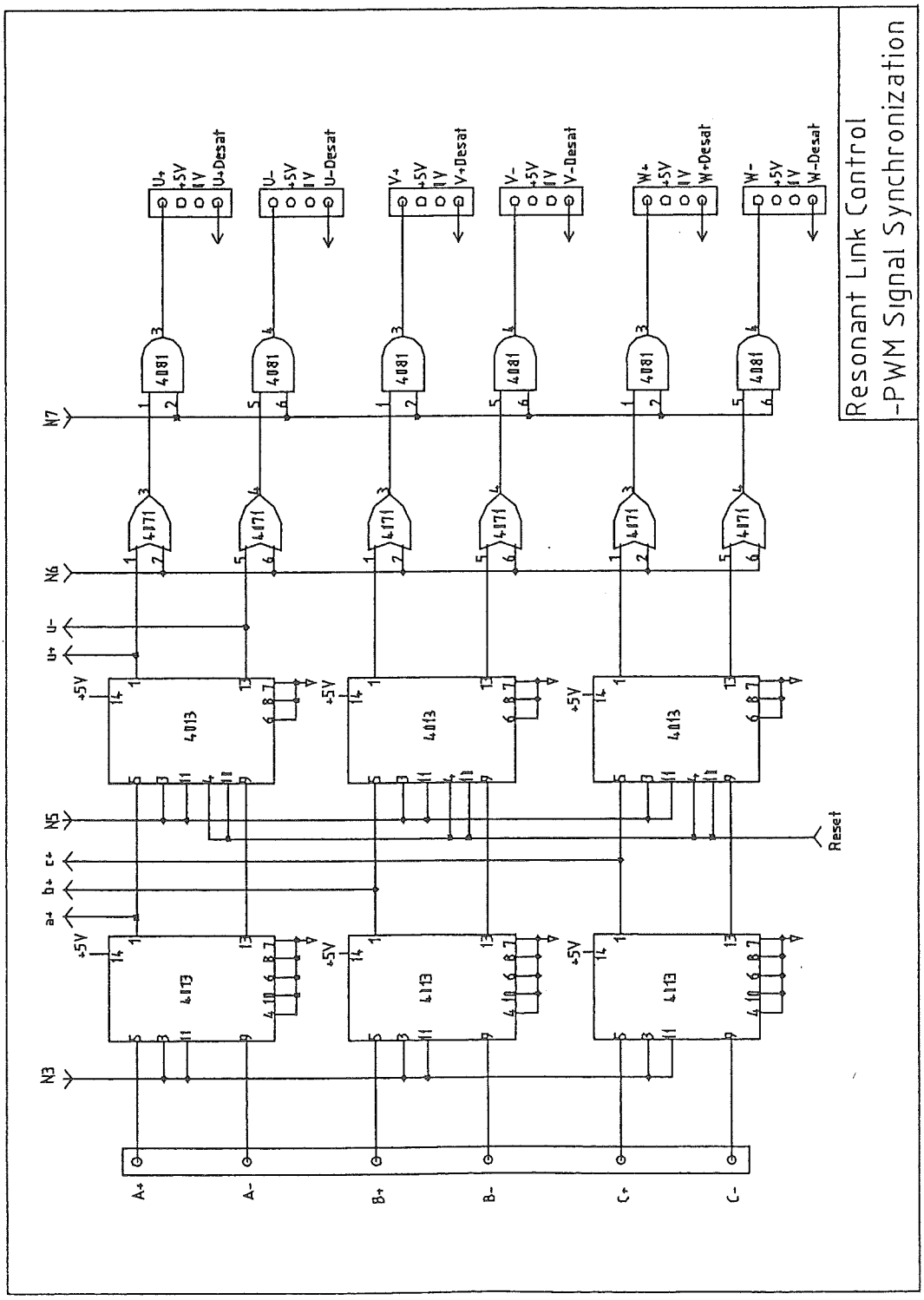
APPENDIX A

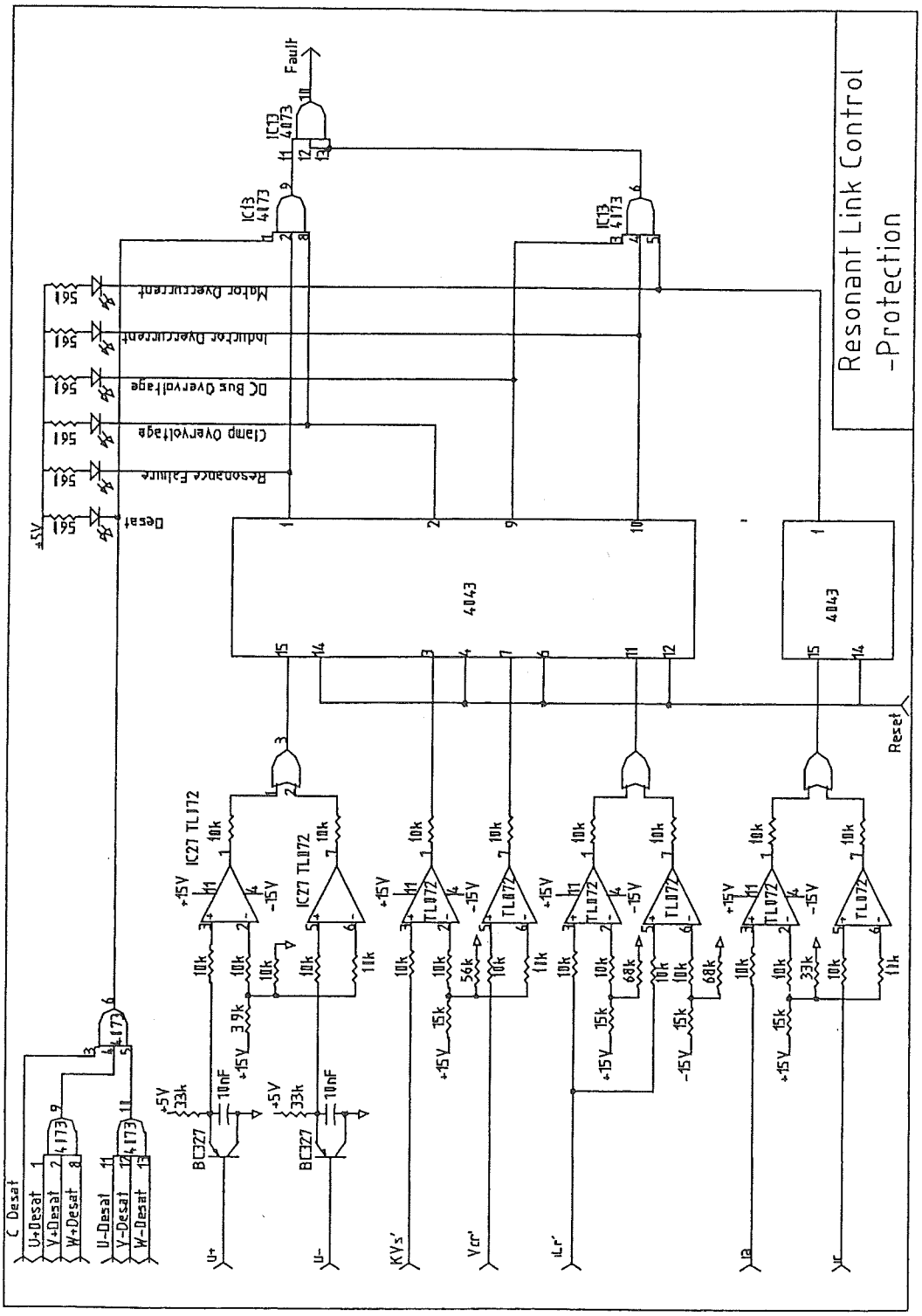
CIRCUIT SCHEMATICS

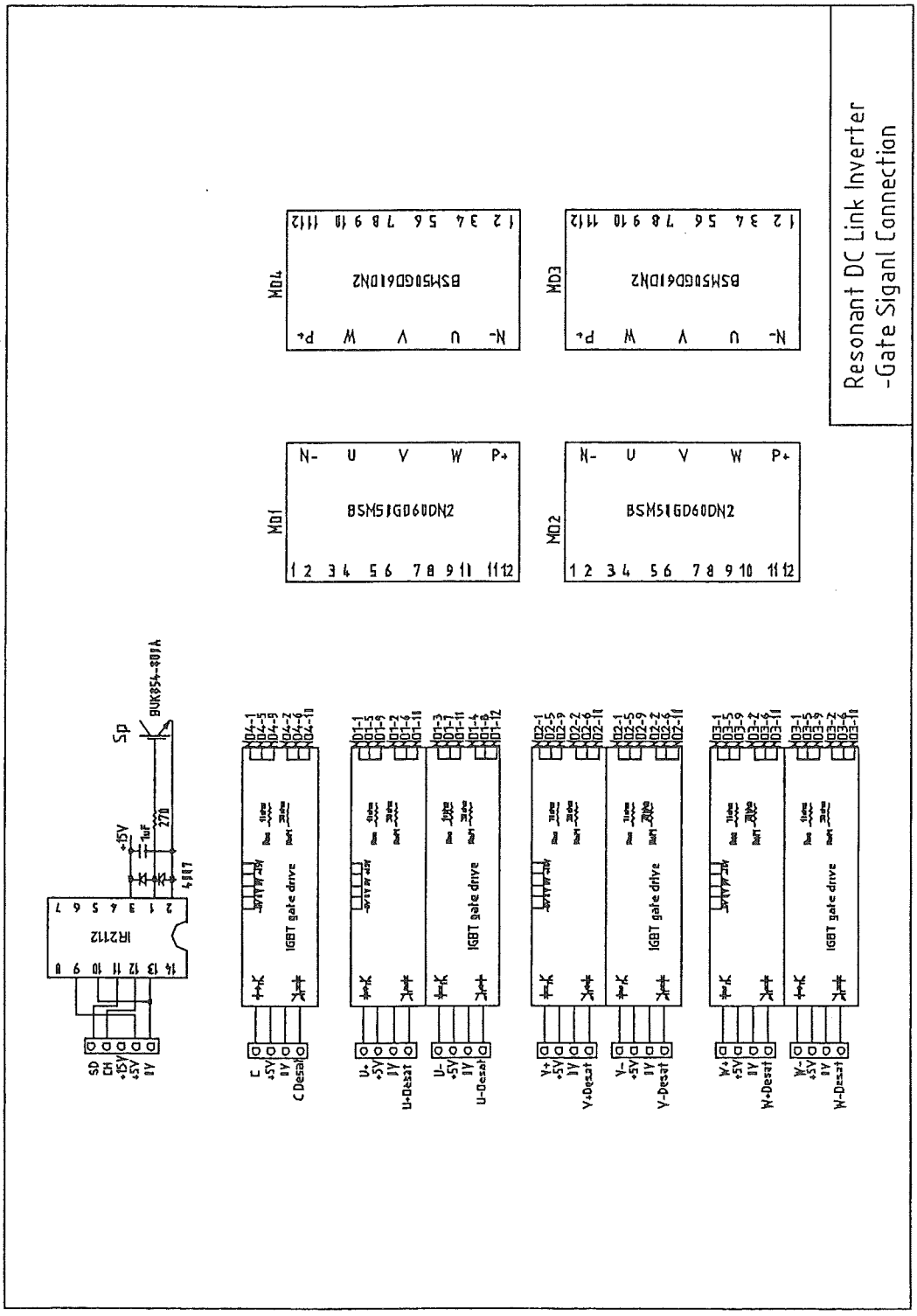


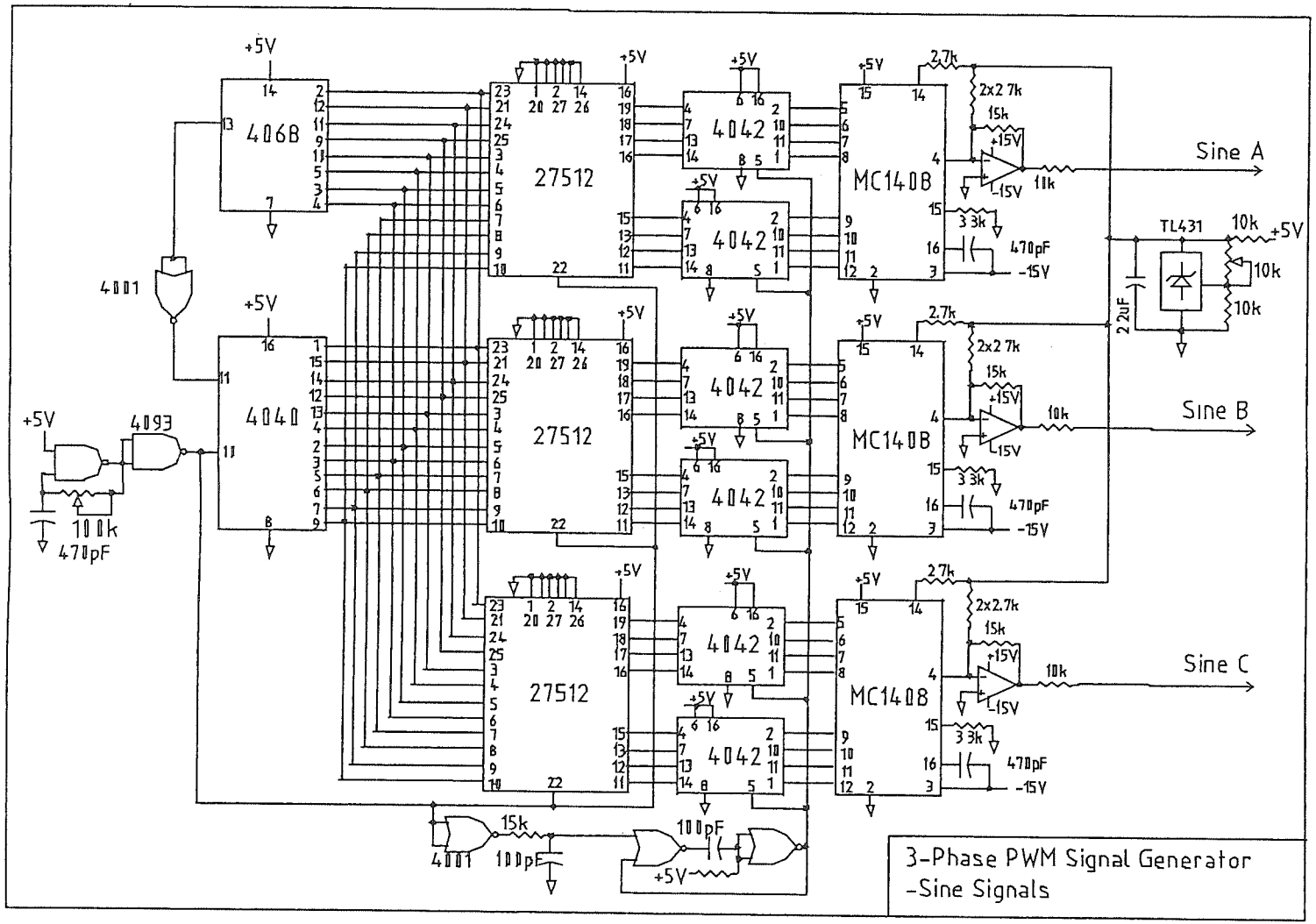

Clamping Voltage
KVs
0V
180k 181k 181k
12k
TL071
+15V
-15V
11k
TL171
N1
KVs'
Vcr'
Bus Voltage
Vcr
0V
LM318
33k 10k
27k
N2
Supply Voltage
Vs
0V
180k 180k 180k
22k
18k 10k
39k
10k
N3
27k 10k
151
N4
Res Inductor Current
0V
iLr
+15V
-15V
331
iLr'
Predicted Current
4151
a+
b+
c+
0.1uF
7.5V
TL071
4.7k
TL074
TL174
Motor Current
330
1V
ia
ic
Resonant Link Control
-Measurement

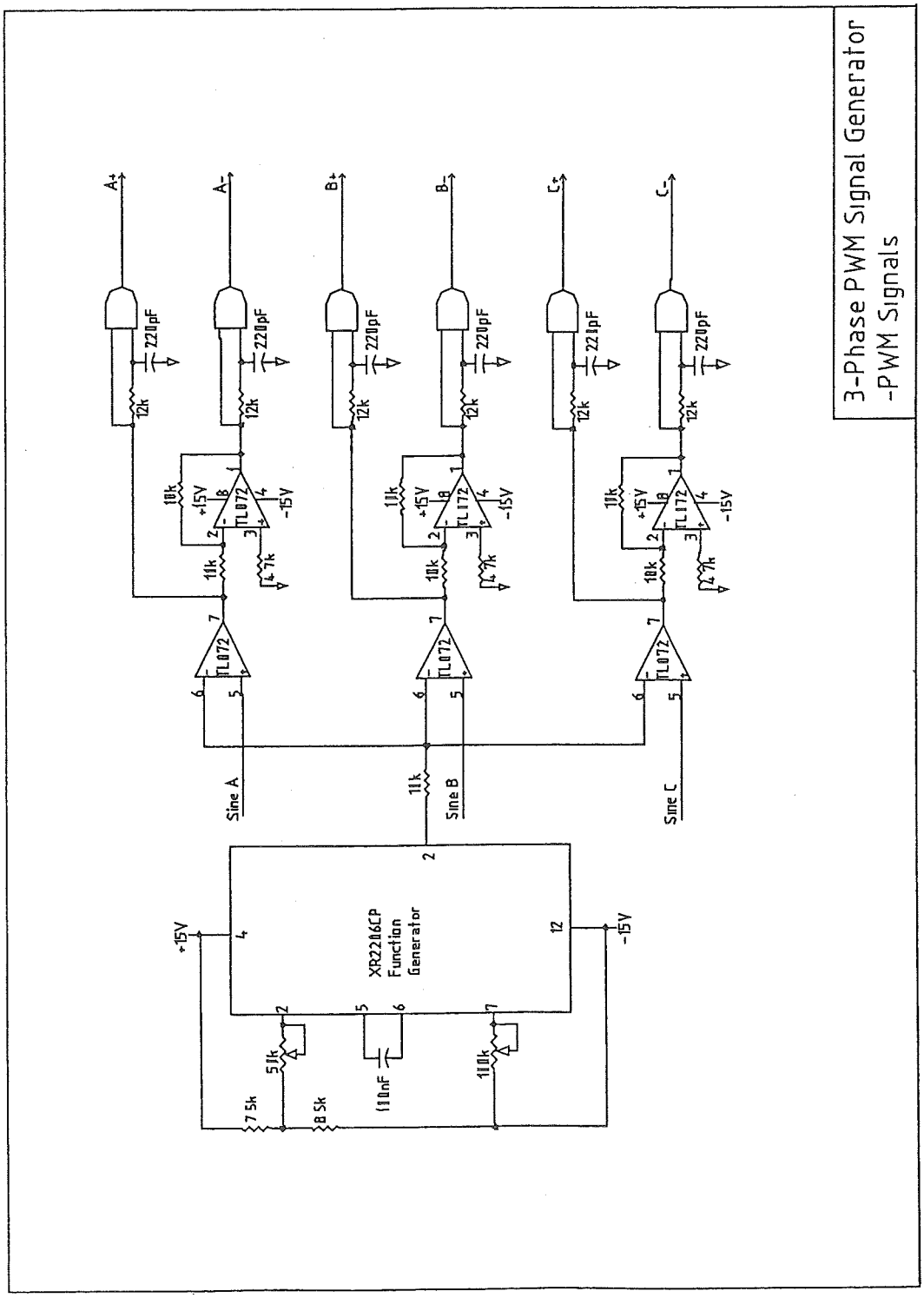

Resonant Link Control
-Charging /Clamping Control
Precharge
SD
FH
+15V
+5V
0V
Clamp Device
C
+5V
0V
C-Desat
N6
N7
Fault
4173
4071
4098
4073
4093
10k
4.7nF
110pF
5.6k
100pF
560/1/271pF
120k
470pF
11k
Q2
Q1
S2
R2
S1
R1
Reset
Start
Stop
N1
N2
N3
N4
N5


Resonant Link Control
-PWM Signal Synchronization
U+
U-
V+
V-
W+
W-
+5V
0V
U+Desat
U-Desat
V+Desat
V-Desat
W+Desat
W-Desat
4081
4071
4013
4013
4013
N7
N6
N5
N3
u+
u-
a+
b+
c+
Reset
A+
A-
B+
B-
C+
C-


Resonant Link Control
-Protection
Fault
IC13
4073
IC13
4173
IC13
4173
Motor Overcurrent
Inductor Overcurrent
DC Bus Overvoltage
Clamp Overvoltage
Resonance Failure
Desat
+5V
561
4043
4043
Reset
IC27 TL072
IC27 TL072
TL072
10k
15k
56k
68k
33k
3.9k
11k
+15V
-15V
+5V
BC327
10nF
C Desat
U+Desat
V+Desat
W+Desat
U-Desat
V-Desat
W-Desat
4173
U+
U-
KVs'
Vcr'
iLr'
Ia
Ic


Resonant DC Link Inverter
-Gate Signal Connection
MD1
BSM51GD60DN2
N- U V W P+
1 2 3 4 5 6 7 8 9 11 11 12
MD2
BSM51GD60DN2
N- U V W P+
1 2 3 4 5 6 7 8 9 10 11 12
MD3
BSM50GD61DN2
N- U V W P+
1 2 3 4 5 6 7 8 9 10 11 12
MD4
BSM50GD61DN2
N- U V W P+
1 2 3 4 5 6 7 8 9 10 11 12
IGBT gate drive
C +5V 11 C Desat
U+ +5V 11 U+Desat
U- +5V 11 U-Desat
V+ +5V 11 V+Desat
V- +5V 11 V-Desat
W+ +5V 11 W+Desat
W- +5V 11 W-Desat
SD CH +15V +5V 11
IR2112
+15V
1uF
270
BUK854-800A
Sp


+5V
406B
27512
4042
MC1408
2.7k
2x2.7k
15k
+15V
-15V
11k
Sine A
TL431
10k
33k
470pF
2.2uF
4001
4040
4093
100k
Sine B
Sine C
100pF
3-Phase PWM Signal Generator
-Sine Signals


3-Phase PWM Signal Generator
-PWM Signals
A+
A-
B+
B-
C+
C-
220pF
12k
10k
11k
18k
4.7k
TL072
+15V
-15V
Sine A
Sine B
Sine C
XR2206CP
Function
Generator
5.1k
110nF
110k
7.5k
8.5k

APPENDIX B

PROGRAM FOR LOSS CALCULATION

```
#include <stdio.h>
#include <math.h>


main()
{
double vs=240,k=1.83,lr=20.45,cr=0.234,q=150,ts=1.1;
double vq=0.85,rq=0.017, vd=1.04,rd=0.012,ta=0.8,b=0.3;
double fc=10,eon=2.3,eoff=5.0,kg=1.2;
double i0=35.35,ma=0.62,pf=0.86,idc;
double fr,w,z,tr,tc,iqm,iqc,icr,ilr,rl;
double iqmavg,iqmrms,idmavg,idmrms;
double iqcavg,iqcrms,idcavg,idcrms;
double pqmcon,pdmcon,pqmsw,pmcon,pm,pm_hard,pqmsw_hard;
double pqccon,pdccon,pqcsw,pccon,pc,pl,pt;
/*************************************************/
fc=fc*1000;
ts=ts*0.000001;
lr=lr*0.000001;
cr=cr*0.000001;
z=sqrt(lr/cr);
w=1.0/sqrt(lr*cr);
ta=ta*0.000001;
/*************************************************/
iqm=vs*ts/lr;
iqc=sqrt(iqm*iqm+(2*k-k*k)*vs*vs/(z*z));
tr=(asin((k-1)*vs/sqrt(z*z*iqm*iqm+vs*vs))+
      asin(vs/sqrt(z*z*iqm*iqm+vs*vs)))/w;
tc=iqc*lr/((k-1)*vs);
fr=1.0/(2*(ts+tr+tc));
/*************************************************/
icr=sqrt(tr*fr*(vs*vs*ts*ts/(lr*lr)+vs*vs/(z*z)));
ilr=sqrt(icr*icr+2*fr*vs*vs*ts*ts*ts/(3*lr*lr)
      +2*fr*lr*iqc*iqc*iqc/(3*(k-1)*vs));
rl=z/q;
idc=0.75*ma*pf*i0;
pl=ilr*ilr*rl+idc*idc*rl;
/*************************************************/
iqmavg=i0*(0.5/3.14159+ma*pf/8);
idmavg=i0*(0.5/3.14159-ma*pf/8);
iqmrms=i0*sqrt(0.125+ma*pf/3/3.14159);
idmrms=i0*sqrt(0.125-ma*pf/3/3.14159);
pqmcon=iqmavg*vq+rq*iqmrms*iqmrms;
pdmcon=idmavg*vd+rd*idmrms*idmrms;
pqmsw=fr/2*z*b*(1-b)*i0*i0*(1/w-sin(w*ta)/(w*w*ta))
      +fr/2*(b*i0*vs+b*b*lr*i0*i0/ta)*(ta/2-(1-cos(w*ta))/(w*w*ta));
pm=6*(pqmcon+pdmcon+pqmsw);
pqmsw_hard=kg*(eon+eoff)*0.001*(vs/300)*(i0/50)*fc/3.14159;
pm_hard=6*(pqmcon+pdmcon+pqmsw_hard);
/*************************************************/
iqcavg=iqc*tc*fr/2.0;
```

```
idcavg=iqcavg;
iqcrms=sqrt(fr*(k-1)*(k-1)*vs*vs*tc*tc*tc/(lr*lr*3));
idcrms=iqcrms;
pqccon=vq*iqcavg+rq*iqcrms*iqcrms;
pdccon=vd*idcavg+rd*idcrms*idcrms;
pqcsw=fr*z*b*(1-b)*iqc*iqc*(1/w-sin(w*ta)/(w*w*ta))+fr*(b*iqc*(k-
      1)*vs+b*b*lr*iqc*iqc/ta)*(ta/2-(1-cos(w*ta))/(w*w*ta));
pc=pqccon+pdccon+pqcsw;
pccon=pqccon+pdccon;
pmcon=6*(pqmcon+pdmcon);
pt=pm+pc+pl;
/*************************************************/
fr=fr*0.001;
lr=lr*1000000;
cr=cr*1000000;
ts=ts*1000000;
tr=tr*1000000;
tc=tc*1000000;
clrscr();
printf("\n\n  ********Power Losses in Hard Switching
      Inverter**********");
printf("\n\n Main Conduction Losses %6.2fW, Main Switching losses
      %6.2fW", pmcon,pqmsw_hard);
printf("\n    Total Losses in HSI     %6.2fW", pm_hard);
printf("\n\n  ********Power Losses in Resonant
      Inverter***************");
printf("\n\n Main Conduction Losses %6.2fW, Main Switching Losses
      %6.2fW", pmcon,pqmsw);
printf("\n Clamp Conduction Losses %6.2fW, Clamp Switching Losses
      %6.2fW", pccon,pqcsw);
printf("\n Inductor Loss  %6.2fW, Total Losses in ACRLI
      %6.2fW",pl,pt);
}
```

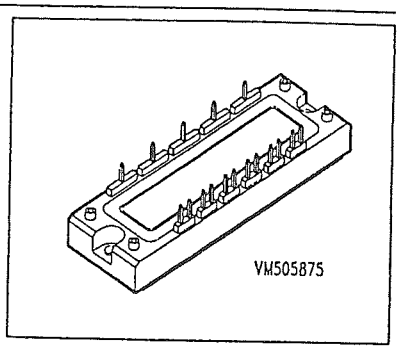
APPENDIX C

SELECTED DATA SHEETS

SIEMENS

BSM 50 GD 60 DN2

IGBT Power Module



- Power module
- 3-phase full-bridge
- Including fast free-wheel diodes
- Package with insulated metal base plate

Type	V_{CE}	I_C	Package	Ordering Code
BSM 50 GD 60 DN2	600V	50A	ECONOPACK 2K	C67076-A2515-A67

Maximum Ratings

Parameter	Symbol	Values	Unit
Collector-emitter voltage	V_{CE}	600	V
Collector-gate voltage R_{GE} = 20 kΩ	V_{CGR}	600	
Gate-emitter voltage	V_{GE}	± 20	
DC collector current T_C = 40 °C	I_C	50	A
Pulsed collector current, t_p = 1 ms T_C = 40 °C	I_{Cpuls}	100	
Power dissipation per IGBT T_C = 25 °C	P_{tot}	200	W
Chip temperature	T_j	+ 150	°C
Storage temperature	T_{stg}	-55 ... + 150	
Thermal resistance, chip case	R_{thJC}	≤ 0.6	K/W
Diode thermal resistance, chip case	R_{thJCD}	≤ 1.5	
Insulation test voltage, t = 1min.	V_{is}	2500	Vac
Creepage distance	-	16	mm
Clearance	-	11	
DIN humidity category, DIN 40 040	-	F	-
IEC climatic category, DIN IEC 68-1	-	55 / 150 / 56	

SIEMENS BSM 50 GD 60 DN2

Electrical Characteristics, at T_j = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static Characteristics					
Gate threshold voltage $V_{GE} = V_{CE}$, I_C = 1 mA	$V_{GE(th)}$	4.5	5.5	6.5	V
Collector-emitter saturation voltage V_{GE} = 15 V, I_C = 50 A, T_j = 25 °C V_{GE} = 15 V, I_C = 50 A, T_j = 125 °C	$V_{CE(sat)}$	- -	2.1 2.2	2.7 2.8	
Zero gate voltage collector current V_{CE} = 600 V, V_{GE} = 0 V, T_j = 25 °C	I_{CES}	-	-	1.5	mA
Gate-emitter leakage current V_{GE} = 25 V, V_{CE} = 0 V	I_{GES}	-	-	100	nA
AC Characteristics					
Transconductance V_{CE} = 20 V, I_C = 50 A	g_{fs}	10	-	-	S
Input capacitance V_{CE} = 25 V, V_{GE} = 0 V, f = 1 MHz	C_{iss}	-	2.8	-	nF
Output capacitance V_{CE} = 25 V, V_{GE} = 0 V, f = 1 MHz	C_{oss}	-	0.3	-	
Reverse transfer capacitance V_{CE} = 25 V, V_{GE} = 0 V, f = 1 MHz	C_{rss}	-	0.2	-	

SIEMENS BSM 50 GD 60 DN2

Electrical Characteristics, at T_j = 25 °C, unless otherwise specified

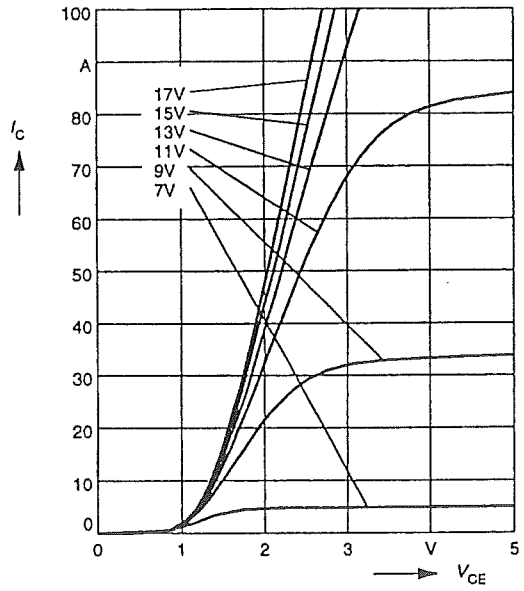
Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Switching Characteristics, Inductive Load at T_j = 125 °C					
Turn-on delay time V_{CC} = 300 V, V_{GE} = 15 V, I_C = 50 A R_{Gon} = 22 Ω	$t_{d(on)}$	-	60	-	ns
Rise time V_{CC} = 300 V, V_{GE} = 15 V, I_C = 50 A R_{Gon} = 22 Ω	t_r	-	80	-	
Turn-off delay time V_{CC} = 300 V, V_{GE} = -15 V, I_C = 50 A R_{Goff} = 22 Ω	$t_{d(off)}$	-	330	-	
Fall time V_{CC} = 300 V, V_{GE} = -15 V, I_C = 50 A R_{Goff} = 22 Ω	t_f	-	550	-	
Free-Wheel Diode					
Diode forward voltage I_F = 50 A, V_{GE} = 0 V, T_j = 25 °C I_F = 50 A, V_{GE} = 0 V, T_j = 125 °C	V_F	- -	2 1.8	- -	V
Reverse recovery time I_F = 50 A, V_R = -300 V, V_{GE} = 0 V dI_F/dt = -500 A/µs, T_j = 125 °C	t_{rr}	-	0.2	-	µs
Reverse recovery charge I_F = 50 A, V_R = -300 V, V_{GE} = 0 V dI_F/dt = -500 A/µs T_j = 25 °C T_j = 125 °C	Q_{rr}	- -	2.8 5	- -	µC

SIEMENS BSM 50 GD 60 DN2

Typ. output characteristics

$I_C = f(V_{CE})$

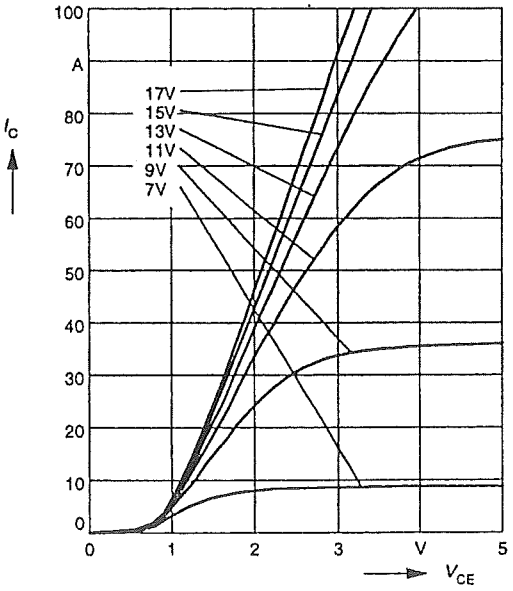
parameter: $t_p = 80\ \mu s$, $T_j = 25\ °C$



Typ. output characteristics

$I_C = f(V_{CE})$

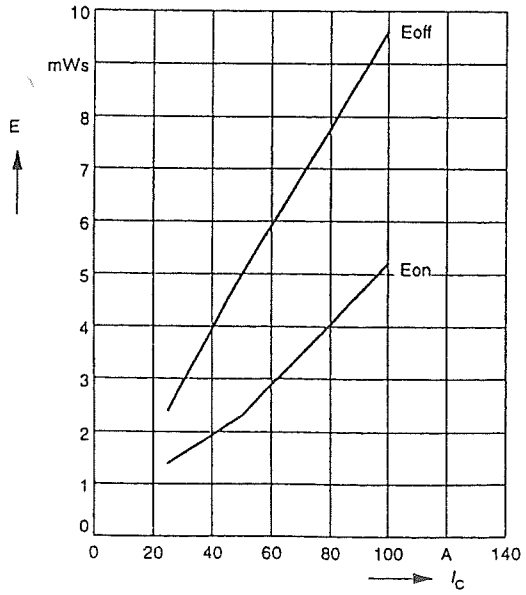
parameter: $t_p = 80\ \mu s$, $T_j = 125\ °C$



Typ. switching losses

$E = f(I_C)$, inductive load, $T_j = 125°C$

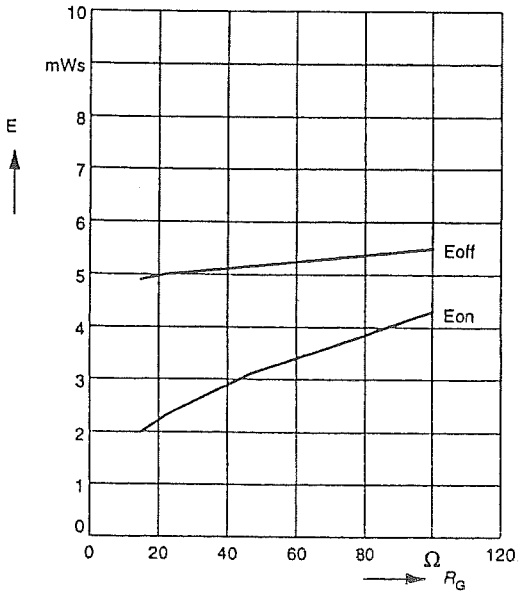
par.: $V_{CE} = 300\ V$, $V_{GE} = \pm 15\ V$, $R_G = 22\ \Omega$



Typ. switching losses

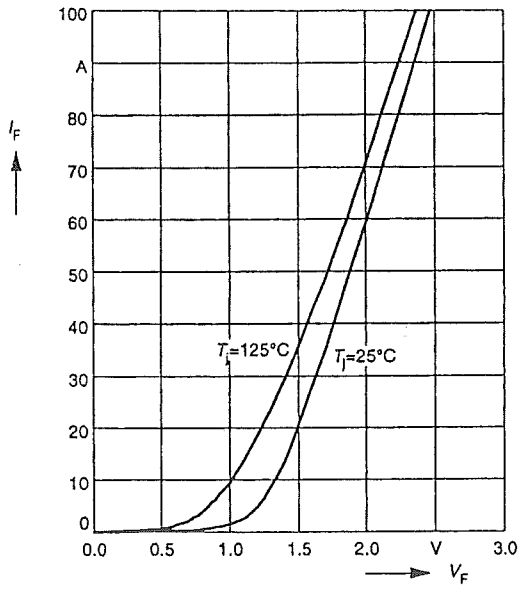
$E = f(R_G)$, inductive load, $T_j = 125°C$

par.: $V_{CE} = 300V$, $V_{GE} = \pm 15\ V$, $I_C = 50\ A$

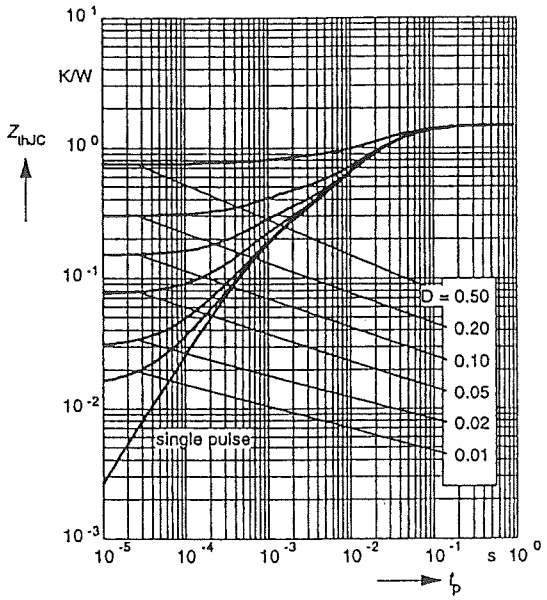


SIEMENS BSM 50 GD 60 DN2

Forward characteristics of fast recovery reverse diode $I_F = f(V_F)$
parameter: T_j



Transient thermal impedance Diode
$Z_{th\,JC} = f(t_p)$
parameter: $D = t_p / T$



PM 114/93
Core

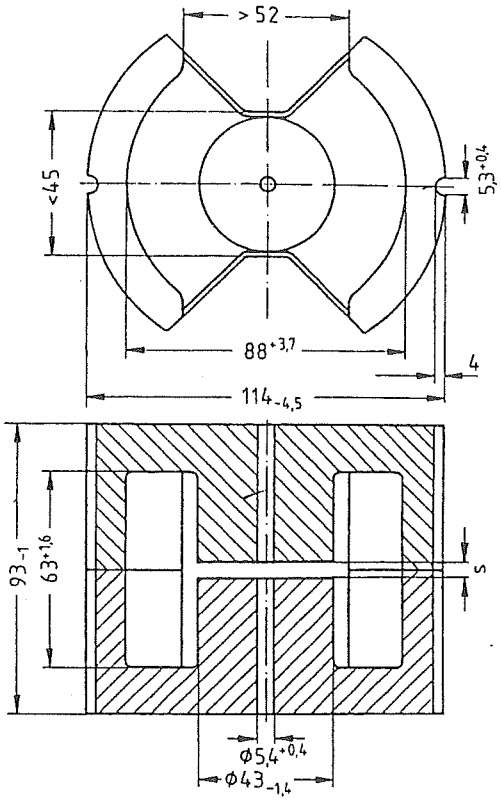
B 65733

- In accordance with DIN 41989
- For power transformers > 1 kW (20 kHz)

Magnetic characteristics (per set)

$\Sigma l/A$	=	0,116	mm^{-1}
l_e	=	200	mm
A_e	=	1720	mm^2
A_{min}	=	1380	mm^2
V_e	=	344000	mm^3

Approx. weight 1940 g/set



Dimensions in mm

Material	A_L value nH	Tolerance %	s approx. mm	μ_e	Ordering code	PU Sets
Gapped						
N 27	630	±3	3,8	58	B65733-A630-A27	1
	1000		2,4	92	B65733-A1000-A27	
	2500	±5	0,70	231	B65733-A2500-J27	
	6300	±15	0,22	581	B65733-A6300-L27	
Ungapped						
N 27	16000	+30/−20		1480	B65733-A-R27 □	1

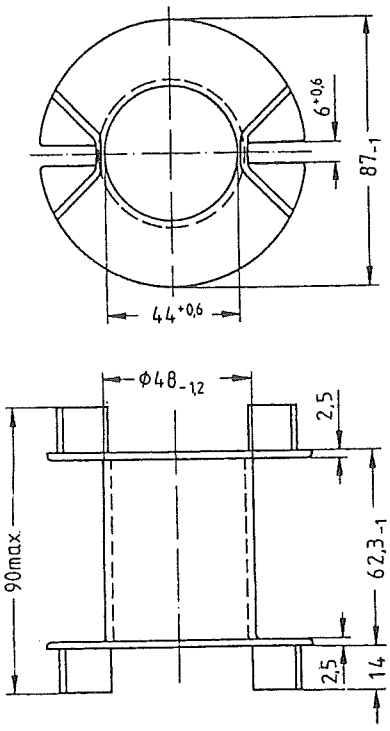
PM 114/93
Accessories

B 65734

Coil former

- In accordance with DIN 41990
- Made of polyphenylene sulphide (UL 94 V-0, thermal class of insulating material in acc. with IEC 85: F), color code brown
- For winding details refer to page 72

Sections	A_N mm²	l_N mm	A_R value μΩ	Approx. weight g	Ordering code	PU Items
1	1070	210	6,75	42	B65734-B1000-T1	5



Dimensions in mm